Technical Handbook

MOSFETS

FERRANTI
Semiconductors

THE QUEEN'S AWARD FOR EXPORT ACHIEVEMENT

1/10/86/10

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MOSFETs

Most devices contained in this publication are also available as individual data sheets

Further information on Ferranti Electronics products may be obtained by filling in the attached reply card below.

FERRANTI ELECTRONICS LIMITED
Fields New Road, Chadderton, Oldham OL9 8NP, England

Please send data on the following:

- ☐ Quick Reference Guide (covers complete range of Integrated Circuits and Discrete Semiconductors)
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Send me individual data sheets on the following device types (Ferranti part number)

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Name __________ Title __________

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FERRANTI ELECTRONICS LIMITED
FIELDS NEW ROAD
CHADDERTON
OLDHAM OL9 8NP
ENGLAND

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It is the intention of Ferranti to phase out voltage downgrades from its MOSFET range. Support will be given to all existing design-ins. In the interim, parts lists should be updated to include the prime types. The following product listing, indicating the devices to refer to, has been generated to assist in this task.

NB Ferranti are not withdrawing any products merely offering a better device without any cost penalty.

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FERRANTI MOSFET TECHNOLOGY

Ferranti MOSFET Technology

Introduction

Ferranti MOSFET technology is amongst the world's most advanced. Its MOSFETs are enhancement mode devices (normally off) especially suited to a wide range of switching and amplifying applications where high gain, high frequency and fast switching speed is desired. They combine the current handling capabilities of bipolar transistors with the high input impedance and negative temperature coefficients of FETs.

Having considered the various MOSFET technologies available (ie V groove, U groove, DMOS) Ferranti has adopted a vertical DMOS structure. The advantages of this structure over the others considered may be summarised as:

- Short channel lengths determined by an easily controlled diffusion process for lower on-resistance and increased current density.
- Planar construction simplifies wafer fabrication due to the elimination of etched grooves
- Increased conductance per unit area
- Improved high voltage capability
- Both N and P-channel devices can be easily fabricated
- Compact metallisation for reduced chip size

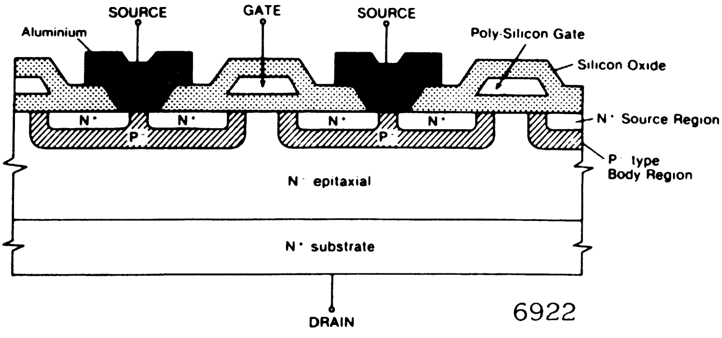
An abundance of terms already exist for individual manufacturers versions of the basic vertical DMOS process eg. HEXFET®, SIPMOS®, TMOS® the main differences being the geometry of the N-type and P-type regions and the interconnections.

Vertical DMOS devices can be fabricated with either an interdigitated or cell geometry.

FERRANTI DMOS PROCESS

Taking an N-channel device as an example. An N^- epitaxial layer is grown on an N^+ substrate. Next a series of P^- body regions are diffused into the epitaxial layer and a poly-silicon gate is embedded in the silicon oxide insulating layer. Source and gate metallisations are deposited on the top surface of the dice and the drain contact made to the bottom surface.

The vertical DMOS process may be considered truly planar as both source and body regions are diffused through a window opened in the poly-silicon layer, without grooves of any kind.



Cross-section of Ferranti vertical DMOS process

Both N and P channel devices utilise the vertical DMOS process. It should be realised, however, that since the resistivity of P-type silicon is much higher than that of an N-type silicon, a P-channel device will require a larger active area to achieve the same on-resistance and current rating. The larger area will mean that parameters related to die area will be different; preventing symmetry in this respect.

Ferranti MOSFET Technology

PROCESS HIGHLIGHTS

- **Poly-silicon gate process** — The poly-silicon gate greatly reduces the possibility of sodium-ion contamination in the gate oxide giving high stability of threshold voltage.

- **Ion implantation** — The use of ion implantation gives stability in the control of threshold voltages in manufacture.

- **Self-aligned gate** — The self-aligned DMOS process allows extremely short channel lengths to be achieved, giving these devices excellent linear transfer characteristics.

- **Planar construction** — The vertical DMOS structure eliminates the need for an isotropically etched V or U-grooves in the surface of the device, giving improved performance and higher voltages.

- **Compact geometries** — Compact transistor chip designs, utilising interdigitated or cell structures optimised for low on-resistance, low capacitance and fast switching speed.

PRODUCT SELECTION TABLES

TABLE 1 : N-CHANNEL SMALL SIGNAL MOSFETS

Part number	BV_{DSS} V	I_D mA	I_{DM} A	$V_{GS(th)}$ V Min.	Max.	@ I_D mA	$R_{DS(on)}$ Ω Max.	@ I_D mA	V_{GS} V	P_D W	Package
ZVN0545A*	450	90	0.6	1	3	1	50	100	10	0.7	E-line
ZVN0545B	450	150	0.6	1	3	1	50	100	10	5	TO-39
ZVN0545L	450	150	0.6	1	3	1	50	100	10	20	TO-220
ZVN0540A*	400	90	0.6	1	3	1	50	100	10	0.7	E-line
ZVN0540B	400	150	0.6	1	3	1	50	100	10	5	TO-39
ZVN0540L	400	150	0.6	1	3	1	50	100	10	20	TO-220
ZVN2535A	350	90	1	1	3	1	35	100	10	0.7	E-line
ZVN2535B	350	250	1	1	3	1	35	100	10	5	TO-39
ZVN2535L	350	250	1	1	3	1	35	100	10	20	TO-220
ZVN0535A*	350	90	0.6	1	3	1	50	100	10	0.7	E-line
ZVN0124A	240	160	2	1	3	1	16	250	10	0.7	E-line
ZVN0124B	240	420	2	1	3	1	16	250	10	5	TO-39
ZVN0124L	240	500	2	1	3	1	16	250	10	20	TO-220
ZVN2120A	200	180	2	1	3	1	10	250	10	0.7	E-line
ZVN2120B	200	460	2	1	3	1	10	250	10	5	TO-39
ZVN2120L	200	500	2	1	3	1	10	250	10	20	TO-220
BS107P	200	120	2	–	–	–	23	25	2.6	0.5	E-line
BS107PT	200	120	2	–	–	–	28	20	2.6	0.5	E-line
ZVN0120A	200	160	2	1	3	1	16	250	10	0.7	E-line
ZVN0120B	200	420	2	1	3	1	16	250	10	5	TO-39
ZVN0120L*	200	500	2	1	3	1	16	250	10	20	TO-220
ZVN3320A	200	100	1	1	3	1	25	100	10	0.625	E-line
ZVN3320B	200	250	1	1	3	1	25	100	10	5	TO-39
ZVN0117TA	170	160	2	–	–	–	23	100	3.3	0.7	E-line
ZVN2110A*	100	320	6	0.8	2.4	1	4	1000	10	0.7	E-line
ZVN2110B*	100	850	6	0.8	2.4	1	4	1000	10	5	TO-39
ZVN2110L	100	1500	6	0.8	2.4	1	4	1000	10	20	TO-220
ZVN3310A	100	200	2	0.8	2.4	1	10	500	10	0.625	E-line
ZVN3310B	100	500	2	0.8	2.4	1	10	500	10	5	TO-39
ZVN1409A	90	10	0.04	0.8	2.4	0.1	250	5	10	0.625	E-line
ZVN4206A	60	600	8	1.3	3	1	1.5	500	5	0.7	E-line
ZVN2106A*	60	450	8	0.8	2.4	1	2	1000	10	0.7	E-line
ZVN2106B*	60	1200	8	0.8	2.4	1	2	1000	10	5	TO-39
ZVN2106L	60	2000	8	0.8	2.4	1	2	1000	10	20	TO-220
ZVN3306A	60	270	3	0.8	2.4	1	5	500	10	0.625	E-line
ZVN3306B	60	750	3	0.8	2.4	1	5	500	10	5	TO-39
VN10LP	60	270	3	0.8	2.5	1	7.5	200	5	0.625	E-line
BS170P	60	270	3	0.8	3	1	5	200	10	0.625	E-line

*BS-CECC approved

SELECTION TABLES

TABLE 2 : P-CHANNEL SMALL SIGNAL MOSFETS

Part number	BV_{DSS}	I_D	I_{DM}	$V_{GS(th)}$ V		@ I_D	$R_{DS(on)}$ Ω	@ I_D	V_{GS}	P_D	Package
	V	mA	A	Min.	Max.	mA	Max.	mA	V	W	
ZVP0545A	−450	−45	−0.4	−1.5	−4.5	−1	150	−50	−10	0.7	E-line
ZVP0545B	−450	−100	−0.4	−1.5	−4.5	−1	150	−50	−10	5	TO-39
ZVP0545L	−450	−100	−0.4	−1.5	−4.5	−1	150	−50	−10	20	TO-220
ZVP0540A	−400	−45	−0.4	−1.5	−4.5	−1	150	−50	−10	0.7	E-line
ZVP0540B	−400	−100	−0.4	−1.5	−4.5	−1	150	−50	−10	5	TO-39
ZVP0540L	−400	−100	−0.4	−1.5	−4.5	−1	150	−50	−10	20	TO-220
ZVP0535A	−350	−50	−0.48	−1.5	−4.5	−1	100	−50	−10	0.7	E-line
ZVP0535B	−350	−120	−0.48	−1.5	−4.5	−1	100	−50	−10	5	TO-39
ZVP0535L	−350	−120	−0.48	−1.5	−4.5	−1	100	−50	−10	20	TO-220
ZVP2120A	−200	−120	−1.2	−1.5	−3.5	−1	25	−150	−10	0.7	E-line
ZVP2120B	−200	−300	−1.2	−1.5	−3.5	−1	25	−150	−10	5	TO-39
ZVP2120L	−200	−300	−1.2	−1.5	−3.5	−1	25	−150	−10	20	TO-220
ZVP0120A	−200	−110	−1	−1.5	−3.5	−1	32	−125	−10	0.7	E-line
ZVP0120B	−200	−250	−1	−1.5	−3.5	−1	32	−125	−10	5	TO-39
ZVP0120L	−200	−250	−1	−1.5	−3.5	−1	32	−125	−10	20	TO-220
ZVP1320A	−200	−70	−0.4	−1.5	−3.5	−1	80	−50	−10	0.625	E-line
ZVP1320B	−200	−100	−0.4	−1.5	−3.5	−1	80	−50	−10	5	TO-39
ZVP2110A*	−100	−230	−3	−1.5	−3.5	−1	8	−375	−10	0.7	E-line
ZVP2110B*	−100	−600	−3	−1.5	−3.5	−1	8	−375	−10	5	TO-39
ZVP2110L	−100	−750	−3	−1.5	−3.5	−1	8	−375	−10	20	TO-220
ZVP3310A	−100	−140	−1.2	−1.5	−3.5	−1	20	−150	−10	0.625	E-line
ZVP3310B	−100	−300	−1.2	−1.5	−3.5	−1	20	−150	−10	5	TO-39
ZVP2106A*	−60	−280	−4	−1.5	−3.5	−1	5	−500	−10	0.7	E-line
ZVP2106B*	−60	−760	−4	−1.5	−3.5	−1	5	−500	−10	5	TO-39
ZVP2106L	−60	−1000	−4	−1.5	−3.5	−1	5	−500	−10	20	TO-220
ZVP3306A	−60	−160	−1.6	−1.5	−3.5	−1	14	−200	−10	0.625	E-line
ZVP3306B	−60	−400	−1.6	−1.5	−3.5	−1	14	−200	−10	5	TO-39
BS250P	−45	−230	−3	−1	−3.5	−1	14	−200	−10	0.7	E-line

*BS-CECC approved

TABLE 3 : LOW THRESHOLD N-CHANNEL MOSFETS

Part number	BV_{DSS}	I_D	I_{DM}	$V_{GS(th)}$ V		@ I_D	$R_{DS(on)}$ Ω	@ I_D	V_{GS}	P_D	Package
	V	mA	A	Min.	Max.	mA	Max.	mA	V	W	
ZVNL535A	350	90	0.8	0.5	1.5	1	40	50	3	0.7	E-line
ZVNL120A	200	180	2	0.5	1.5	1	10	125	3	0.7	E-line

TABLE 4 : SOT-23 MOSFETS

Part number	BV_{DSS} V	I_D mA	I_{DM} A	$V_{GS(th)}$ V Min.	$V_{GS(th)}$ V Max.	@ I_D mA	$R_{DS(on)}$ Ω Max.	@ I_D mA	V_{GS} V	P_D mW	Package marking
N-channel											
ZVN3320F	200	60	1	1	3	1	25	100	10	250	MU
ZVN3310F	100	100	2	0.8	2.4	1	10	500	10	250	MF
ZVN4106F	60	200	3	1.3	3	1	2.5	500	10	250	MZ
ZVN3306F	60	150	3	0.8	2.4	1	5	500	10	250	MC
VN10LF	60	150	3	0.8	2.5	1	7.5	200	5	250	MY
BS170F	60	150	3	0.8	3	1	5	200	10	250	MV
P-channel											
ZVP1320F	−200	−35	−0.4	−1.5	−3.5	−1	80	−50	−10	250	MT
ZVP3310F	−100	−75	−1.2	−1.5	−3.5	−1	20	−150	−10	250	MR
ZVP3306F	−60	−90	−1.6	−1.5	−3.5	−1	14	−200	−10	250	ML
BS250F	−45	−90	−1.6	−1.5	−3.5	−1	14	−200	−10	250	MX

TABLE 5 : MEDIUM POWER N/P CHANNEL MOSFETS

Part number	BV_{DSS} V	I_D A	I_{DM} A	$V_{GS(th)}$ V Min.	$V_{GS(th)}$ V Max.	@ I_D mA	$R_{DS(on)}$ Ω Max.	@ I_D A	V_{GS} V	P_D W	Package
N-channel											
ZVN2224B	240	1.2	6	1	3	2	6	1	10	20	TO-39
ZVN2224L	240	1.2	6	1	3	2	6	1	10	20	TO-220
ZVN2220B	200	1.85	8	1	3	2	2.5	1	10	20	TO-39
ZVN2220L	200	1.85	8	1	3	2	2.5	1	10	20	TO-220
ZVN2210B*	100	3.45	12	1	3	2	0.8	2	10	20	TO-39
ZVN2210L	100	3.45	12	1	3	2	0.8	2	10	20	TO-220
ZVN2206B*	60	4.8	16	1	3	2	0.5	2	10	20	TO-39
ZVN2206L	60	4.8	16	1	3	2	0.5	2	10	20	TO-220
P-channel											
ZVP2220B	−200	−0.9	−4	−1.5	−3.5	−1	12	−0.5	−10	20	TO-39
ZVP2220L	−200	−0.9	−4	−1.5	−3.5	−1	12	−0.5	−10	20	TO-220
ZVP2210B*	−100	−1.5	−6	−1.5	−3.5	−1	3	−0.75	−10	20	TO-39
ZVP2210L	−100	−1.5	−6	−1.5	−3.5	−1	3	−0.75	−10	20	TO-220
ZVP2206B*	−60	−2	−8	−1.5	−3.5	−1	1.6	−1	−10	20	TO-39
ZVP2206L	−60	−2	−8	−1.5	−3.5	−1	1.6	−1	−10	20	TO-220

*BS-CECC approved

SELECTION TABLES

TABLE 6 : TO-220 N-CHANNEL POWER MOSFETS

Part number	BV_{DSS}	I_D	I_{DM}	$V_{GS(th)}$ V		@ I_D	$R_{DS(on)}$ Ω	@ I_D	V_{GS}	P_D
	V	A	A	Min.	Max.	μA	Max.	A	V	W
IRF630	200	9	36	2	4	250	0.4	5	10	75
ZVN3220L	200	8	32	2	4	250	0.5	5	10	75
IRF632	200	8	32	2	4	250	0.6	5	10	75
IRF620	200	5	20	2	4	250	0.8	2.5	10	40
IRF622	200	4	16	2	4	250	1.2	2.5	10	40
IRF631	150	9	36	2	4	250	0.4	5	10	75
IRF633	150	8	32	2	4	250	0.6	5	10	75
IRF621	150	5	20	2	4	250	0.8	2.5	10	40
IRF623	150	4	16	2	4	250	1.2	2.5	10	40
ZVN3210L*	100	14	56	2	4	250	0.18	8	10	75
IRF530	100	14	56	2	4	250	0.18	8	10	75
IRF532	100	12	48	2	4	250	0.25	8	10	75
IRF520	100	8	32	2	4	250	0.3	4	10	40
IRF522	100	7	28	2	4	250	0.4	4	10	40
ZVN3206L*	60	18	72	2	4	250	0.12	10	10	75
IRF531	60	14	56	2	4	250	0.18	8	10	75
IRF533	60	12	48	2	4	250	0.25	8	10	75
IRF521	60	8	32	2	4	250	0.3	4	10	40
IRF523	60	7	28	2	4	250	0.4	4	10	40
IRFZ30+	50	30	80	2	4	250	0.05	16	10	75
IRFZ32+	50	25	60	2	4	250	0.07	16	10	75
IRFZ20+	50	15	60	2	4	250	0.1	9	10	40
IRFZ22+	50	14	56	2	4	250	0.12	9	10	40

* BS-CECC approved
+Advanced information

MOSFET DICE

TABLE 7 : ELECTRICAL PROBE SPECIFICATIONS FOR N-CHANNEL MOSFET DIE

Chip type (size)	Part No.	Maximum Rated V_{DS}	$R_{DS(on)}$ max	@ I_D	V_{DS}	Max I_{DSS} @ rated V_{DS}	Max I_{GSS} @ $V_{GS}=20V$	$V_{GS(th)}$ min	$V_{GS(th)}$ max	@ I_D	Data sheet for packaged device
14 (.023" × .023")	ZVN1409	90V	250Ω	0.1mA	10V	1μA	100nA	0.8V	2.4V	0.1mA	G-139
21 (.042" × .042")	ZVN0124	240V	16Ω	250mA	10V	10μA	20nA	1V	3V	1mA	G-119
	ZVN2120	200V	10Ω	250mA	10V	10μA	20nA	1V	3V	1mA	G-163
	ZVN2110	100V	4Ω	1A	10V	1μA	20nA	0.8V	2.4V	1mA	G-155
	ZVN2106	60V	2Ω	1A	10V	0.5μA	20nA	0.8V	2.4V	1mA	G-147
22 (.062" × .072")	ZVN2224	240V	6Ω	1A	10V	10μA	20nA	1V	3V	2mA	G-195
	ZVN2220	200V	2.5Ω	1A	10V	10μA	20nA	1V	3V	2mA	G-187
	ZVN2210	100V	0.8Ω	2A	10V	2μA	20nA	1V	3V	2mA	G-179
	ZVN2206	60V	0.5Ω	2A	10V	2μA	20nA	1V	3V	2mA	G-171
25 (.041" × .043")	ZVN0545	450V	50Ω	100mA	10V	10μA	20nA	1V	3V	1mA	G-137
	ZVN2535	350V	35Ω	100mA	10V	10μA	20nA	1V	3V	1mA	G-197
33 (.030" × .030")	ZVN3320	200V	25Ω	100mA	10V	10μA	100nA	1V	3V	1mA	G-245
	ZVN3310	100V	10Ω	500mA	10V	1μA	20nA	0.8V	2.4V	1mA	G-237
	ZVN3306	60V	5Ω	500mA	10V	0.5μA	20nA	0.8V	2.4V	1mA	G-229

TABLE 8 : ELECTRICAL PROBE SPECIFICATIONS FOR P-CHANNEL MOSFET DIE

Chip type (size)	Part No.	Maximum Rated V_{DS}	$R_{DS(on)}$ max	@ I_D	V_{DS}	Max I_{DSS} @ rated V_{DS}	Max I_{GSS} @ $V_{GS}=20V$	$V_{GS(th)}$ min	$V_{GS(th)}$ max	@ I_D	Data sheet for packaged device
21 (.042" × .042")	ZVP2120	−200V	25Ω	−150mA	−10V	−10μA	−20nA	−1.5V	−3.5V	−1mA	G-295
	ZVP2110	−100V	8Ω	−375mA	−10V	−1μA	−20nA	−1.5V	−3.5V	−1mA	G-287
	ZVP2106	−60V	5Ω	−500mA	−10V	−0.5μA	−20nA	−1.5V	−3.5V	−1mA	G-279
22 (.062" × .072")	ZVP2220	−200V	12Ω	−500mA	−10V	−10μA	−20nA	−1.5V	−3.5V	−1mA	G-319
	ZVP2210	−100V	3Ω	−750mA	−10V	−2μA	−20nA	−1.5V	−3.5V	−1mA	G-311
	ZVP2206	−60V	1.6Ω	−1mA	−10V	−2μA	−20nA	−1.5V	−3.5V	−1mA	G-303
25 (.041" × .043")	ZVP0545	−450V	150Ω	−50mA	−10V	−20μA	−20nA	−1.5V	−4.5V	−1mA	G-269
	ZVP0535	−350V	100Ω	−50mA	−10V	−20μA	−100nA	−1.5V	−4.5V	−1mA	G-259
33 (.030" × .030")	ZVP1320	−200V	80Ω	−50mA	−10V	−10μA	−20nA	−1.5V	−3.5V	−1mA	G-271
	ZVP3310	−100V	20Ω	−150mA	−10V	−1μA	−20nA	−1.5V	−3.5V	−1mA	G-335
	ZVP3306	−60V	14Ω	−200mA	−10V	−0.5μA	−20nA	−1.5V	−3.5V	−1mA	G-327

MOSFET DICE

SHIPPING OPTIONS

MOSFET dice are supplied in two shipping options as follows:

OPTION A (suffix W):

Wafer (slice) form. Probed wafers are tested to the major d.c. parameters, rejects being automatically inked. The unscribed wafers are shipped in specially designed plastic boxes offering the highest degree of protection, preventing movement and breakages.

OPTION B (suffix D):

Dice carrying diaphragm. For the supply of individual dice Ferranti has developed a dice carrying diaphragm. After a wafer has been probed (rejects inked) and sawn, sections of the wafer (dependent upon the size of die) are laid on low adhesive film and cracked. This film is then stretched over a 4″ ring and held in position by a second ring pressed over the first. In this way the die are separated whilst retaining the relative position they held in wafer form, with each die orientated in the same way, ie. geometries aligned.

ORDERING INFORMATION

MOSFET dice should be ordered by quoting the part number as stated in tables 7 and 8, the suffix D or W depending on the shipping option, and finally the shipping option.

EXAMPLES

ZVN2110W — Option A

or

ZVN2110D — Option B

APPROVALS

TABLE 9 : FERRANTI PART NUMBER/BS-CECC CROSS REFERENCE

Part number	BS-CECC No.
ZVN0120L	50012-020
ZVN0535A	50012-019
ZVN0540A	50012-019
ZVN0545A	50012-019
ZVN2106A	50012-018
ZVN2106B	50012-031
ZVN2110A	50012-018
ZVN2110B	50012-031
ZVN2206B	50012-032

Part number	BS-CECC No.
ZVN2210B	50012-032
ZVN3206L	50012-021
ZVN3210L	50012-021
ZVP2106A	50012-033
ZVP2106B	50012-034
ZVP2110A	50012-033
ZVP2110B	50012-034
ZVP2206B	50012-035
ZVP2210B	50012-035

TABLE 10 : BS-CECC/FERRANTI PART NUMBER CROSS REFERENCE

BS-CECC No.	Part number
50012-018	ZVN2106A ZVN2110A
50012-019	ZVN0535A ZVN0540A ZVN0545A
50012-020	ZVN0120L
50012-021	ZVN3206L ZVN3210L
50012-031	ZVN2106B ZVN2110B

BS-CECC No.	Part number
50012-032	ZVN2206B ZVN2210B
50012-033	ZVP2106A ZVP2110A
50012-034	ZVP2106B ZVP2110B
50012-035	ZVP2206B ZVP2210B

ORDERING INFORMATION

When ordering BS-CECC approved products the following prefix/suffix apply.

EXAMPLES:

E-Line devices (prefix BSI)
BSIZVN2110A to BS-CECC 50012-018

TO-39 devices (suffix BS)
ZVN2210BBS to BS-CECC 50012-032

TO-220 devices (suffix BS)
ZVN3210LBS to BS-CECC 50012-021

DEVICE RATINGS, SPECIFICATIONS AND CHARACTERISTICS

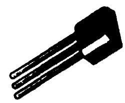
This section contains the range of MOSFET'S offered by Ferranti. Some changes to earlier published data have been made. The data presented here supersedes all previous specifications

N-channel enhancement mode vertical DMOS FET

BS107P

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BS107P	200V	0.12A	23Ω

BS107P

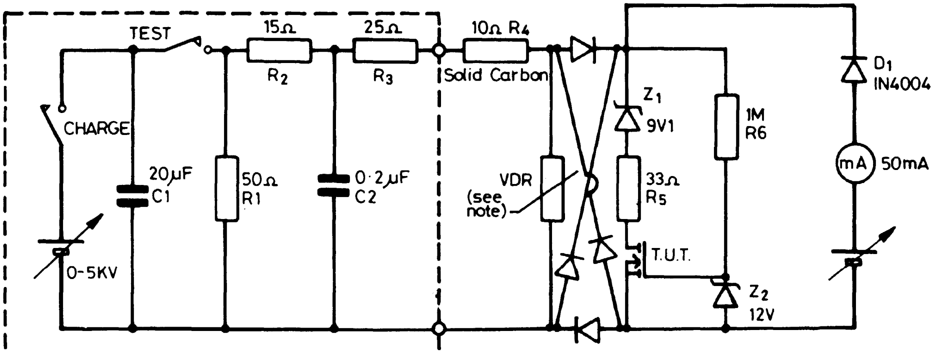
ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.12	A
I_{DM}	Pulse drain current	2	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	230	–	V	$I_D = 100\mu A$, $V_{GS} = 0V$
I_{GSS}	Gate body leakage	–	–	10	nA	$V_{GS} = 15V$, $V_{DS} = 0V$
I_{DSS}	Drain cut-off current	–	–	30	nA	$V_{DS} = 130V$, $V_{GS} = 0V$
I_{DSX}		–	–	1	μA	$V_{DS} = 70V$, $V_{GS} = 0.2V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	15	23	Ω	$I_D = 25mA$, $V_{GS} = 2.6V$
		–	–	30	Ω	$I_D = 100mA$, $V_{GS} = 5V$

(1)Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.



Note: VDR types - Mullard 2322 594 11012
Siemens S10V S07K 75
Matsushita ER2-C070K 10

The transistor under test should withstand a surge applied via above circuit when C1 is charged to 1.5kV.

Fig. 1 Surge test circuit

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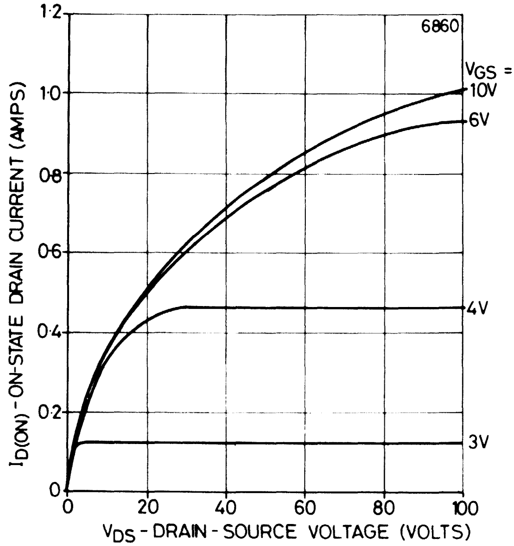


Fig. 2 Typical output characteristics

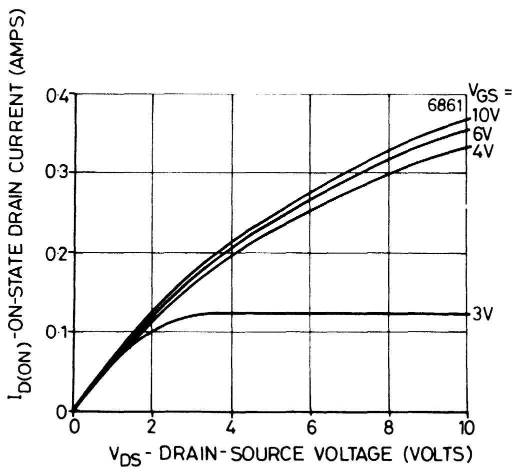


Fig. 3 Typical saturation characteristics

BS107P

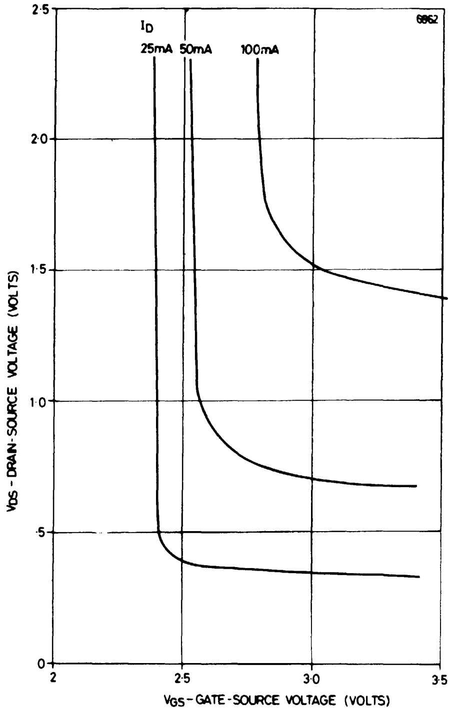


Fig. 4 Typical voltage saturation characteristics

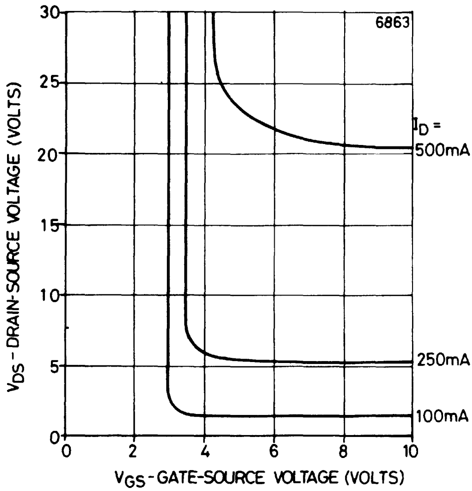


Fig. 5 Typical voltage saturation characteristics

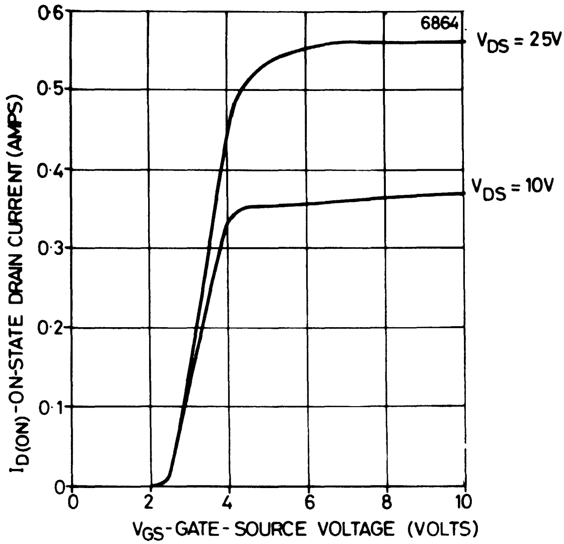


Fig. 6 Typical transfer characteristics

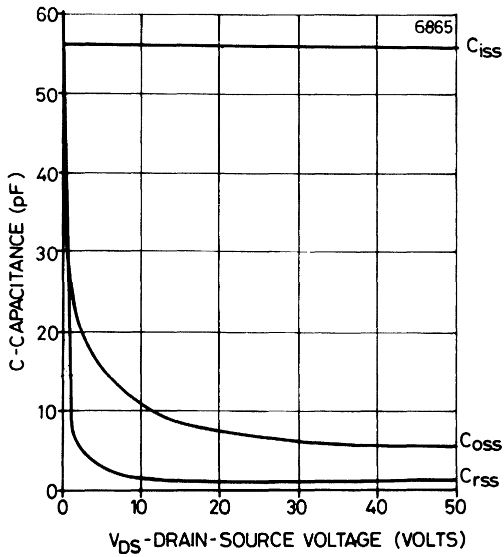


Fig. 7 Typical capacitance v drain-source voltage

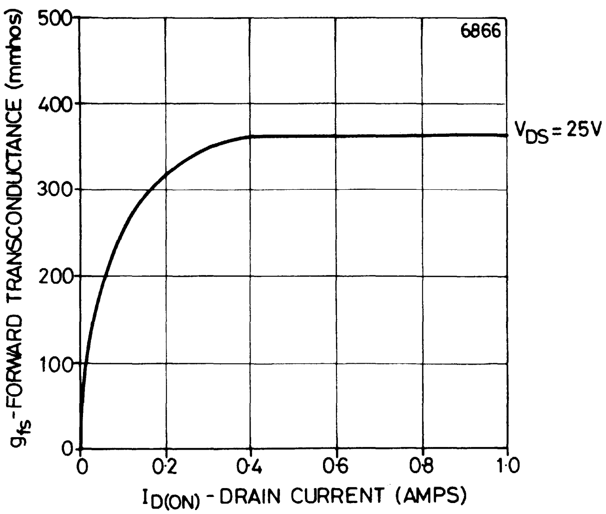


Fig. 8 Typical transconductance v drain current

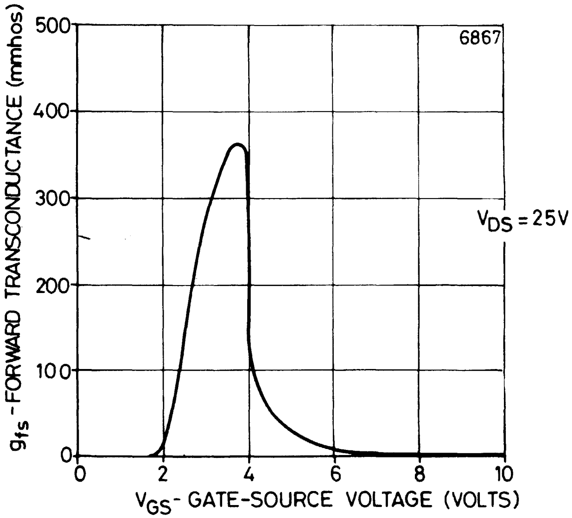


Fig. 9 Typical transconductance v gate-source voltage

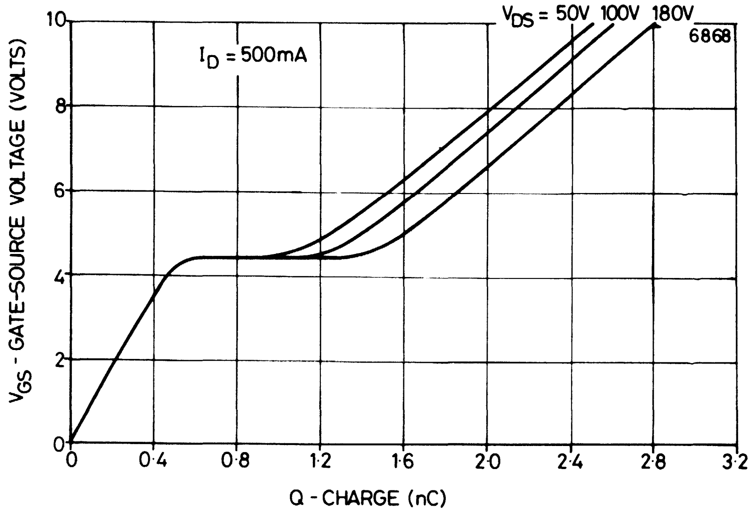


Fig. 10 Typical gate charge v gate-source voltage

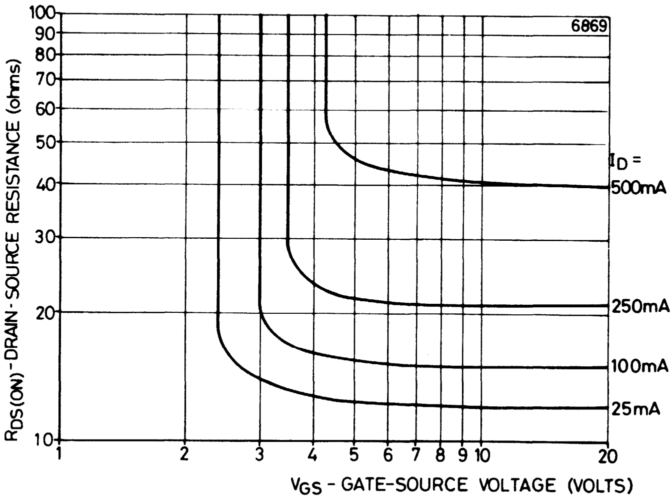


Fig. 11 Typical on-resistance v gate-source voltage

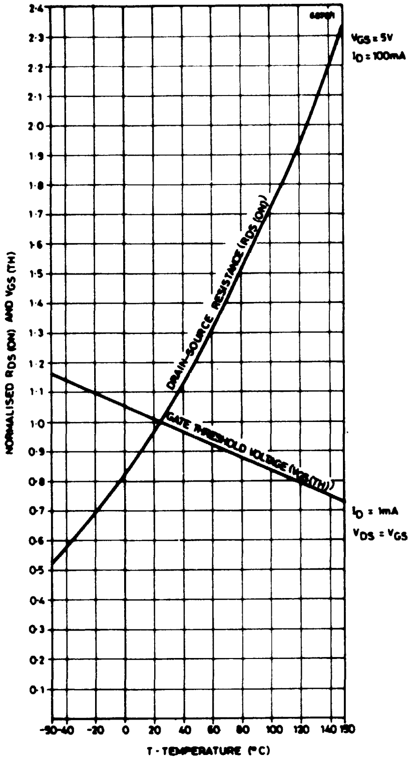


Fig. 12 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

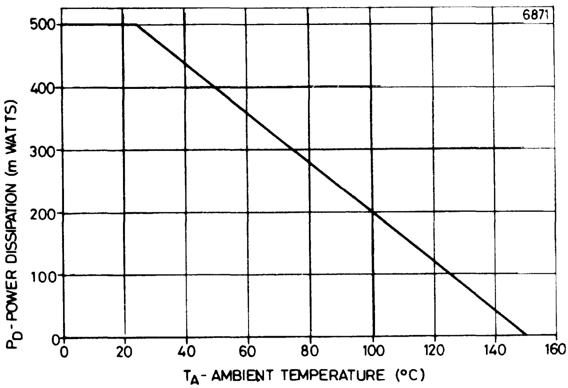


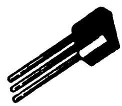
Fig. 13 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

BS107PT

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BS107PT	200V	0.12A	28Ω

BS107PT

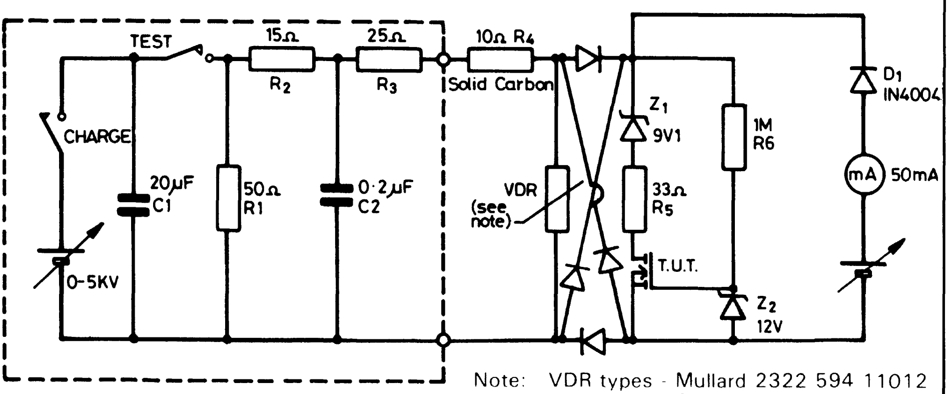
ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.12	A
I_{DM}	Pulse drain current	2	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.5	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	230	–	V	$I_D = 100\mu A$, $V_{GS} = 0V$
I_{GSS}	Gate body leakage	–	–	10	nA	$V_{GS} = 15V$, $V_{DS} = 0V$
I_{DSS}	Drain cut-off current	–	–	30	nA	$V_{DS} = 130V$, $V_{GS} = 0V$
I_{DSX}		–	–	1	μA	$V_{DS} = 70V$, $V_{GS} = 0.2V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	15	28	Ω	$I_D = 20mA$, $V_{GS} = 2.6V$
		–	–	30	Ω	$I_D = 100mA$, $V_{GS} = 2.7V$

(1)Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.



Note: VDR types - Mullard 2322 594 11012
Siemens S10V S07K 75
Matsushita ER2-C070K 10

The transistor under test should withstand a surge applied via above circuit when C1 is charged to 1.5kV.

Fig. 1 Surge test circuit

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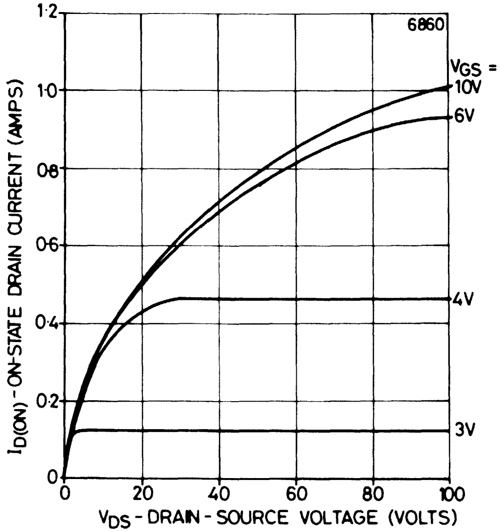


Fig. 2 Typical output characteristics

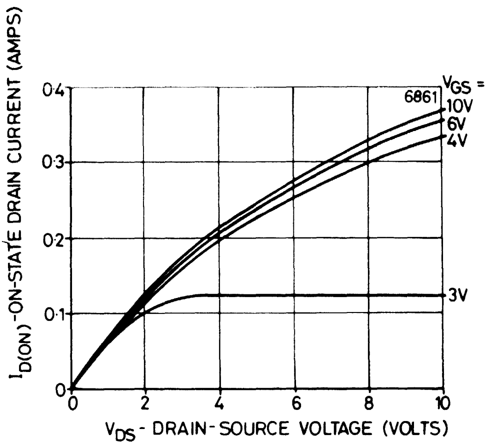


Fig. 3 Typical saturation characteristics

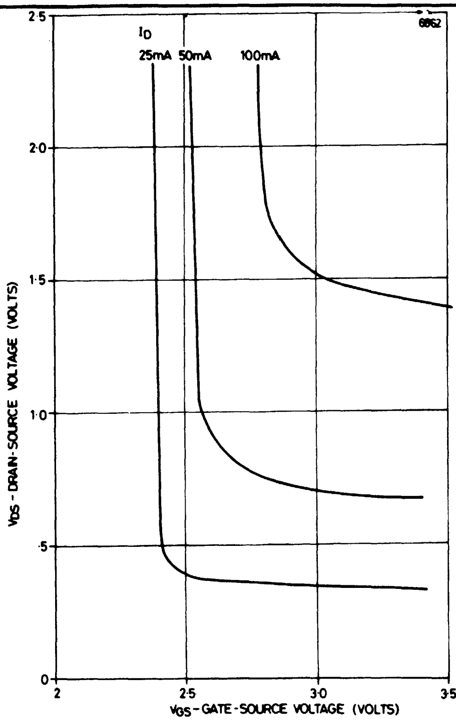


Fig. 4 Typical voltage saturation characteristics

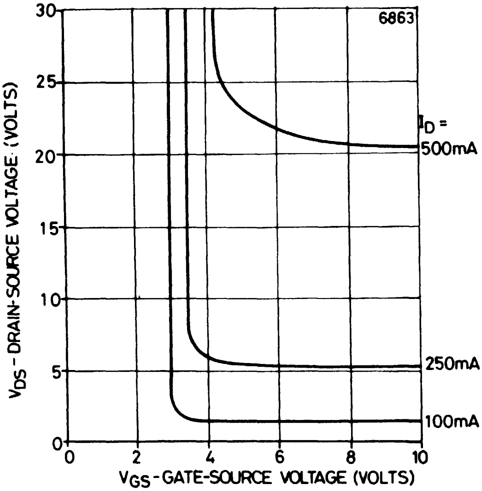


Fig. 5 Typical voltage saturation characteristics

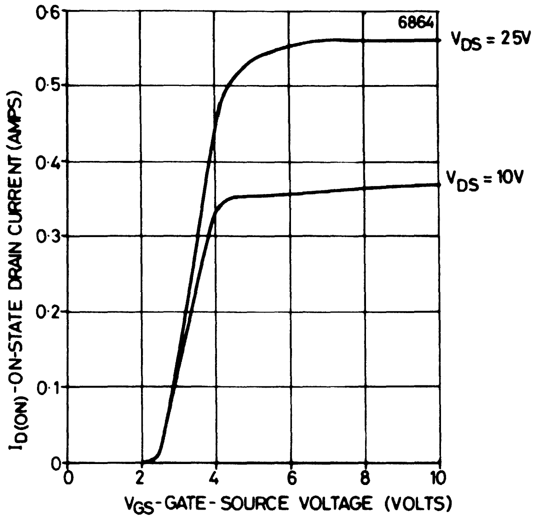


Fig. 6 Typical transfer characteristics

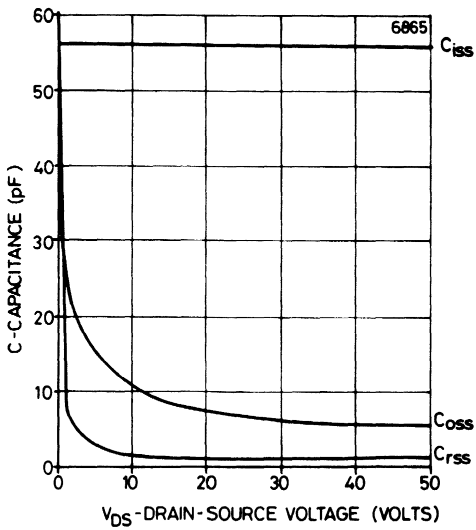


Fig. 7 Typical capacitance v drain-source voltage

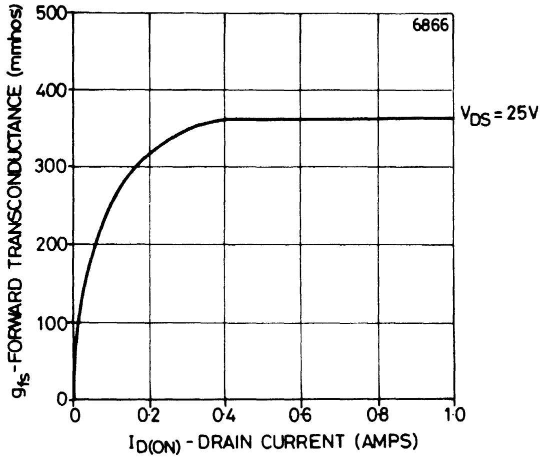


Fig. 8 Typical transconductance v drain current

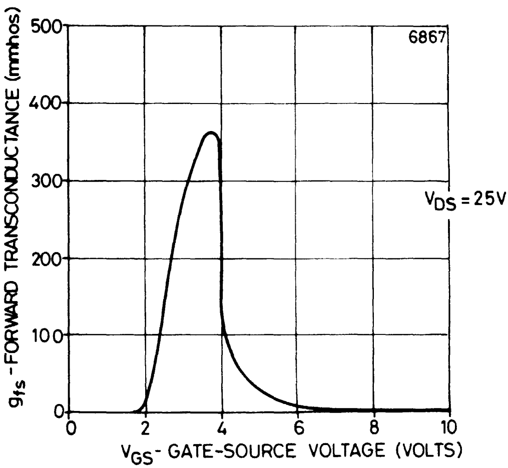


Fig. 9 Typical transconductance v gate-source voltage

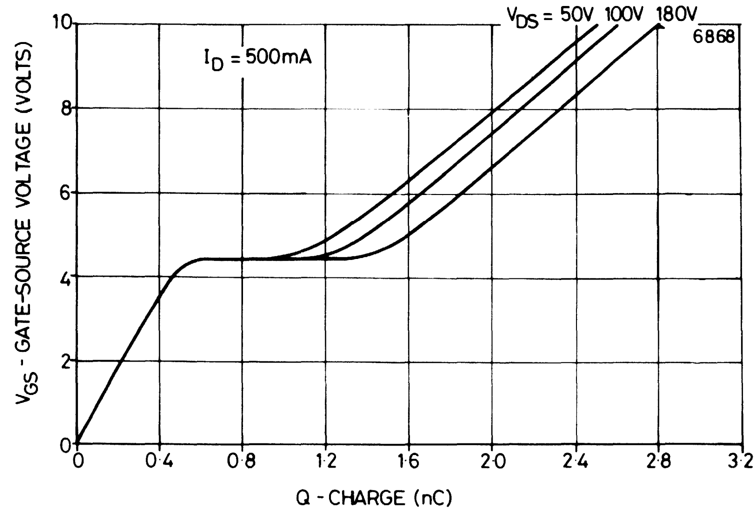


Fig. 10 Typical gate charge v gate-source voltage

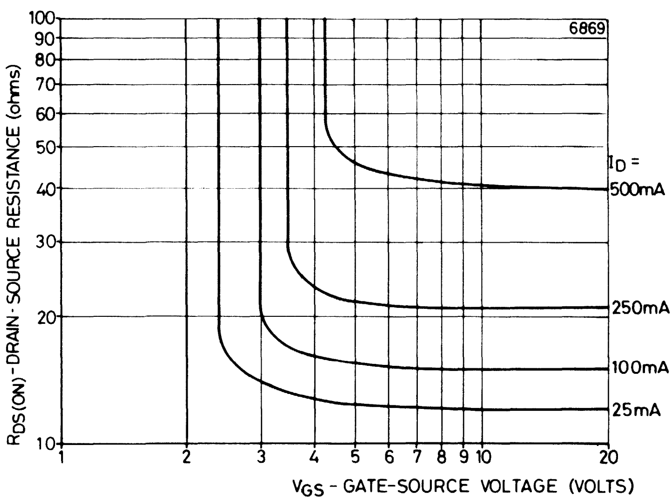


Fig. 11 Typical on-resistance v gate-source voltage

BS107PT

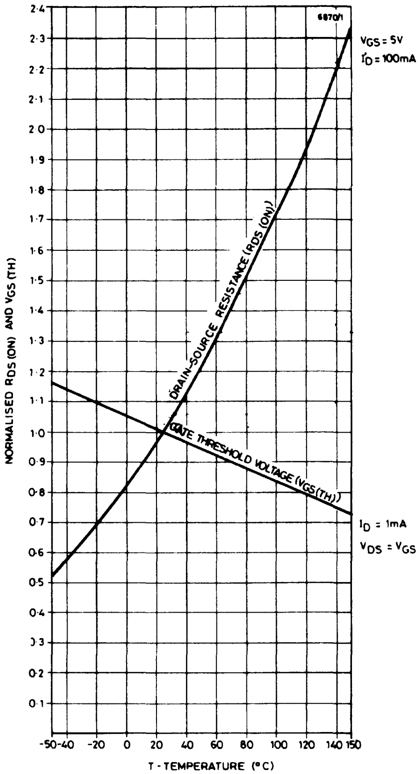


Fig. 12 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

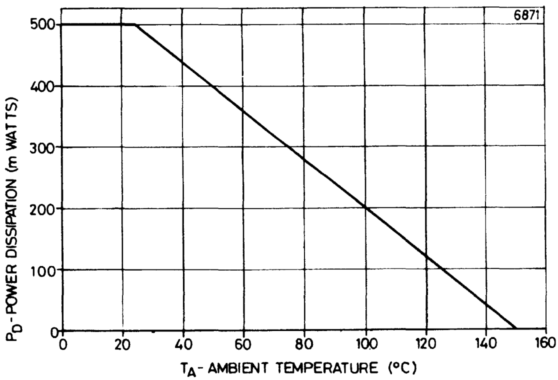


Fig. 13 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

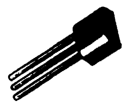
BS170

FEATURES

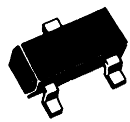
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.



E-LINE (TO-92)
SUFFIX P



SOT-23
SUFFIX F

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BS170P	60V	0.27A	5Ω
BS170F	60V	0.15A	5Ω

BS170

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	SOT-23	Units
V_{DS}	Drain-source voltage	60	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.27	0.15	A
I_{DM}	Pulse drain current	3	3	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.25	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	90	–	V	$I_D = 100\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	10	nA	$V_{GS} = 15V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	0.5	μA	$V_{DS} = 25V$, $V_{GS} = 0V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	5	Ω	$I_D = 200mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	–	200	–	mS	$V_{DS} = 10V$, $I_D = 200mA$
C_{iss}	Input capacitance (2)	–	60	–	pF	$V_{DS} = 10V$, $V_{GS} = 0V$ f = 1MHz
$t_{(on)}$	Turn-on time (2) (3)	–	–	10	ns	$V_{DD} \approx 15V$, $I_D = 600mA$
$t_{(off)}$	Turn-off time (2) (3)	–	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator.

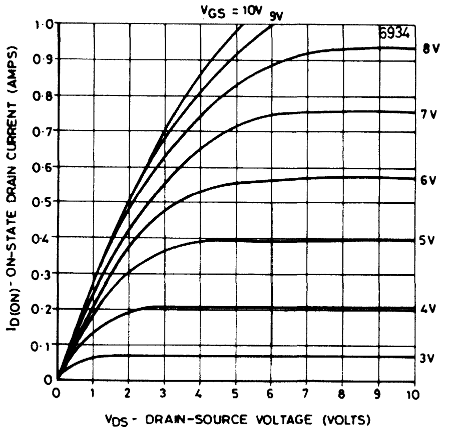


Fig. 1 Typical saturation characteristics

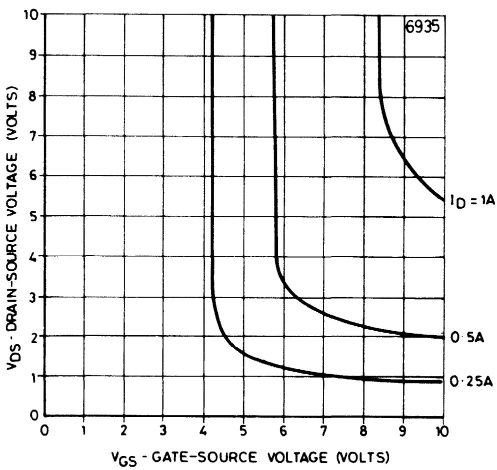


Fig. 2 Typical voltage saturation characteristics

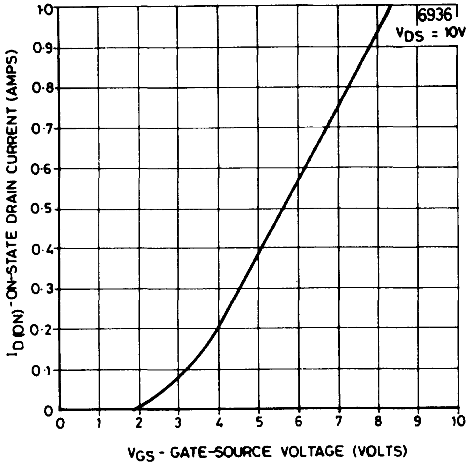


Fig. 3 Typical transfer characteristics

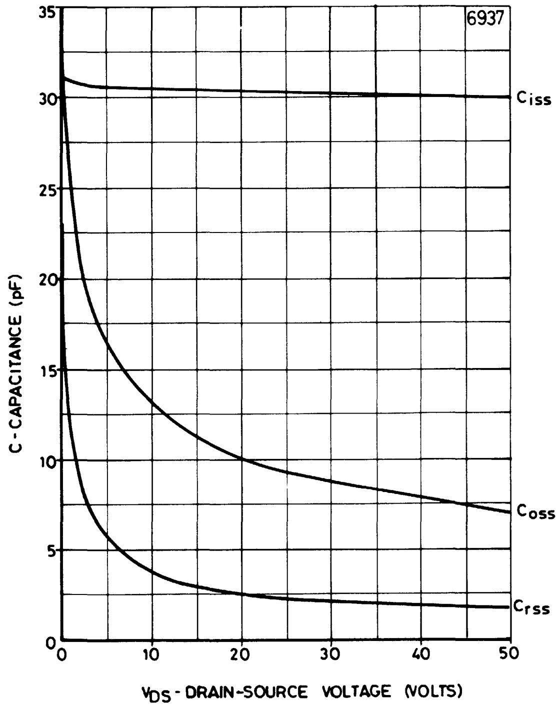


Fig. 4 Typical capacitance v drain-source voltage

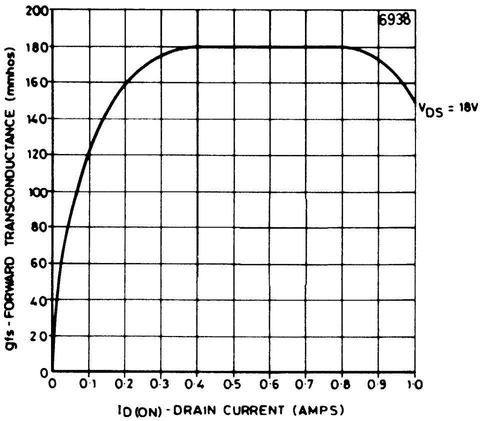


Fig. 5 Typical transconductance v drain current

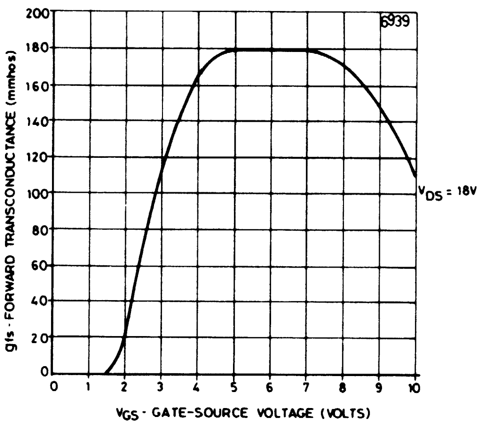


Fig. 6 Typical transconductance v gate-source voltage

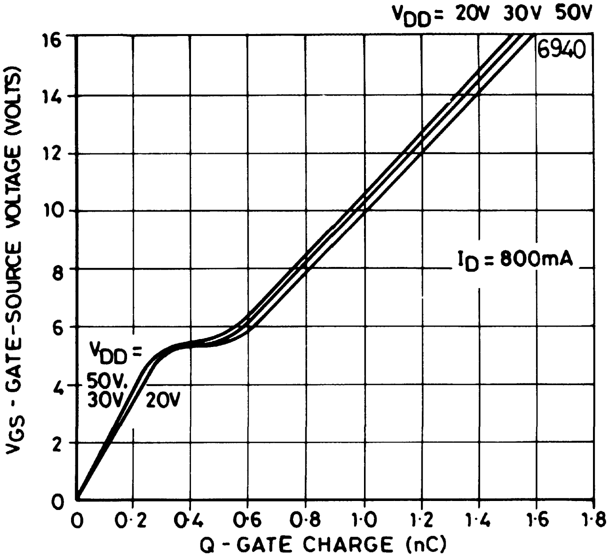


Fig. 7 Typical gate charge v gate-source voltage

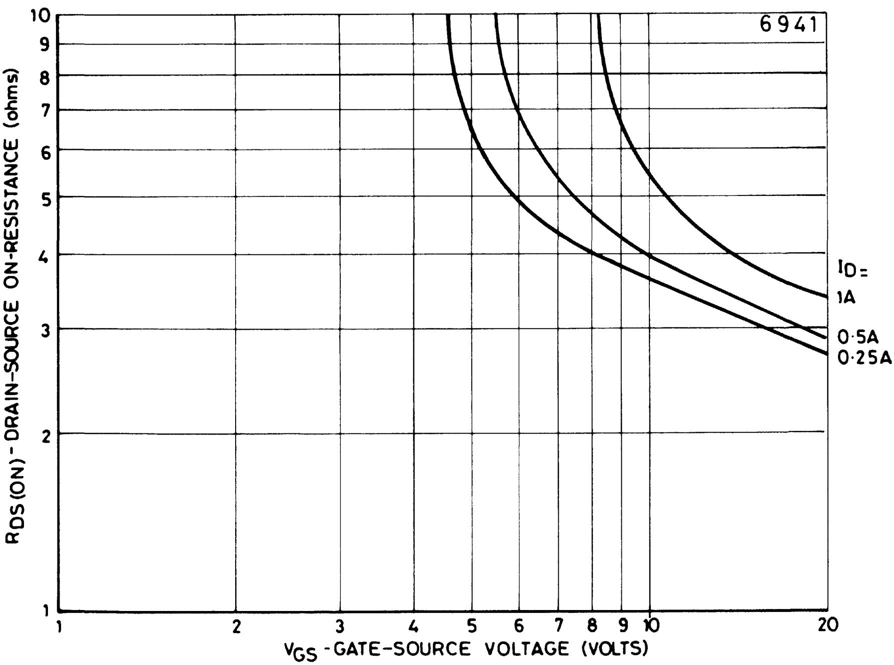


Fig. 8 Typical on-resistance v gate-source voltage

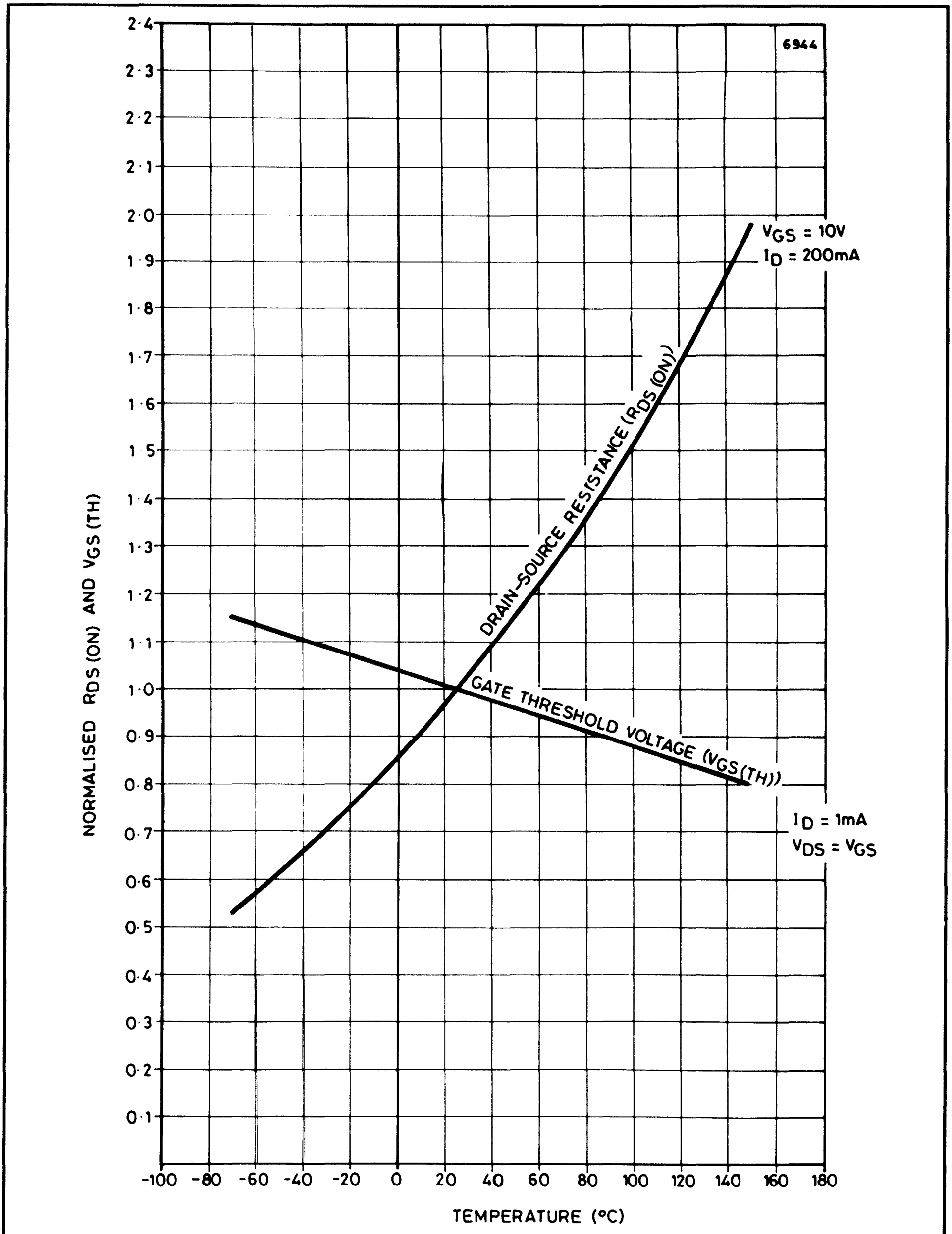


Fig. 9 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

BS170

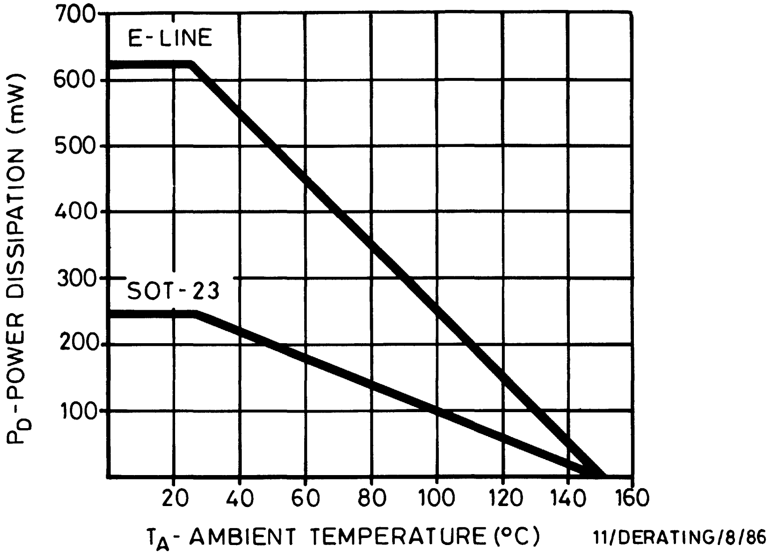


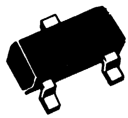
Fig. 10 Power v temperature derating curve (ambient)

P-channel enhancement mode vertical DMOS FET

BS250F

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



SOT-23

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BS250F	−45V	−0.09A	14Ω

BS250F

ABSOLUTE MAXIMUM RATINGS

Parameters		SOT-23	Unit
V_{DS}	Drain-source voltage	−45	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.09	A
I_{DM}	Pulse drain current	−1.6	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.25	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−45	−70	–	V	$I_D = -100\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1	–	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	−20	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	−0.5	μA	$V_{DS} = -25V$, $V_{GS} = 0V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	9	14	Ω	$I_D = -200mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	–	90	–	mS	$V_{DS} = -10V$, $I_D = -200mA$
C_{iss}	Input capacitance (2)	–	25	–	pF	$V_{DS} = -10V$, $V_{GS} = 0V$ f = 1MHz
$t_{d(on)}$	Turn-on delay time (2) (3)	–	–	10	ns	$V_{DD} \approx -25V$, $I_D = -200mA$
t_r	Rise time (2) (3)	–	–	10	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	–	10	ns	
t_f	Fall time (2) (3)	–	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

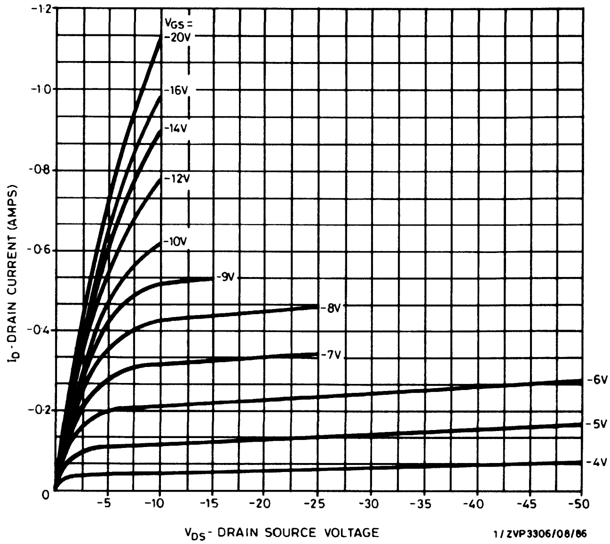


Fig. 1 Typical output characteristics

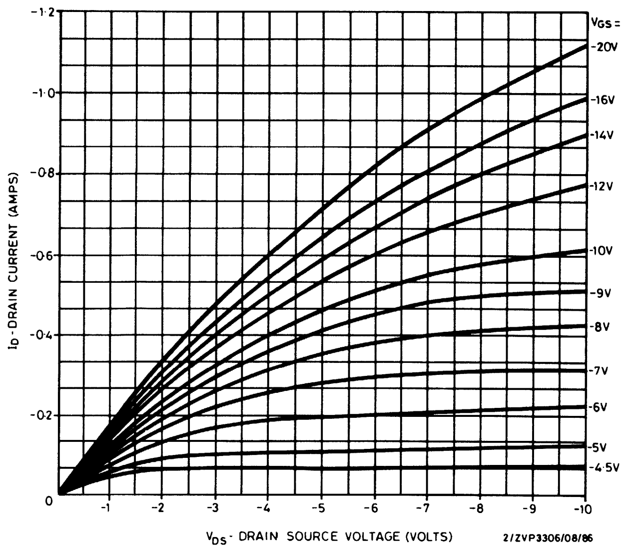


Fig. 2 Typical saturation characteristics

BS250F

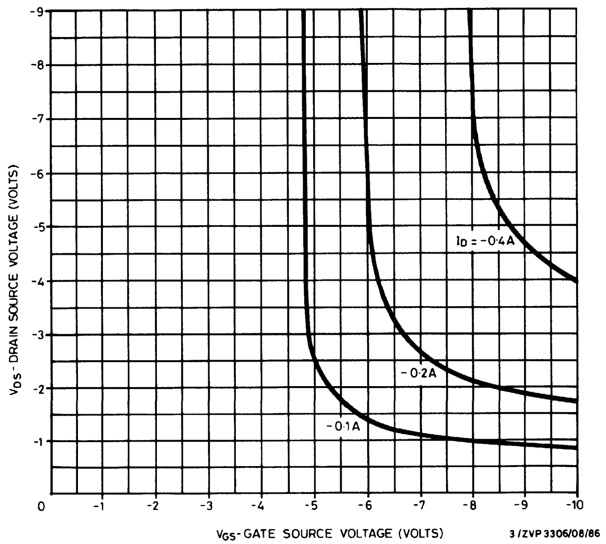


Fig. 3 Typical voltage saturation characteristics

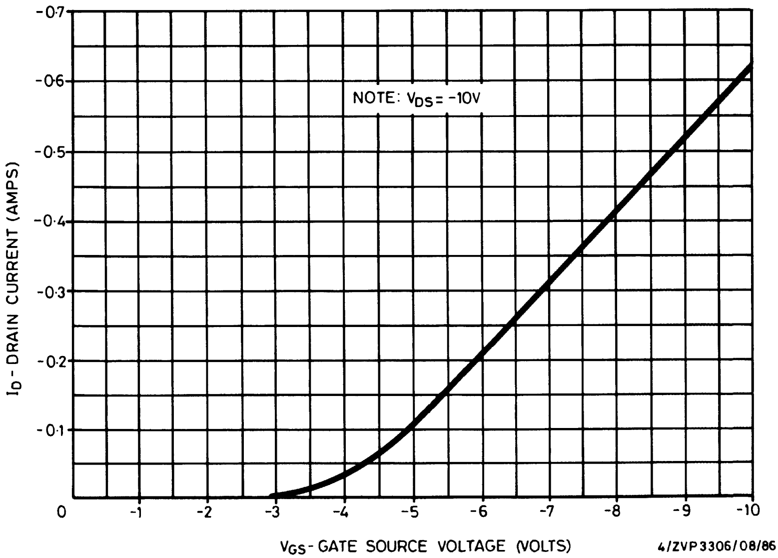


Fig. 4 Typical transfer characteristics

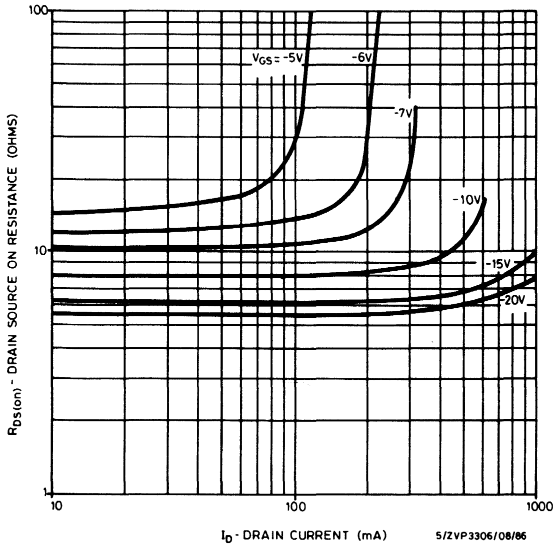


Fig. 5 Typical on-resistance v drain current

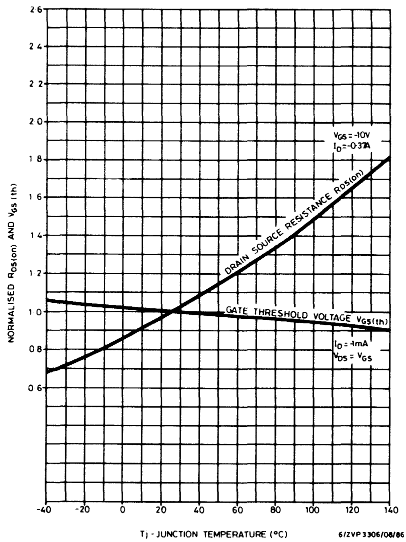


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

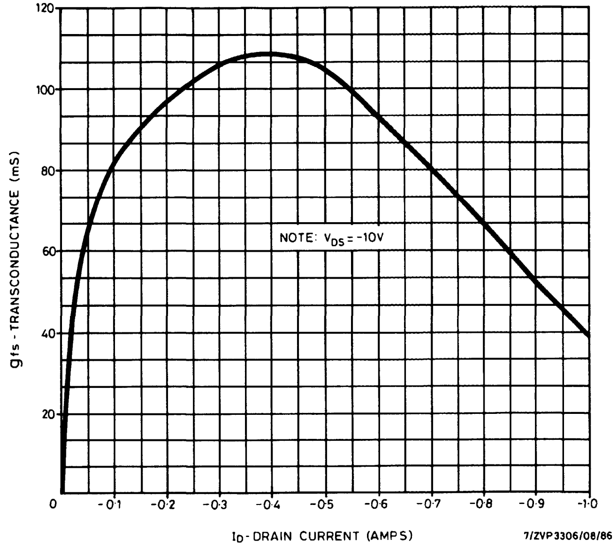


Fig. 7 Typical transconductance v drain current

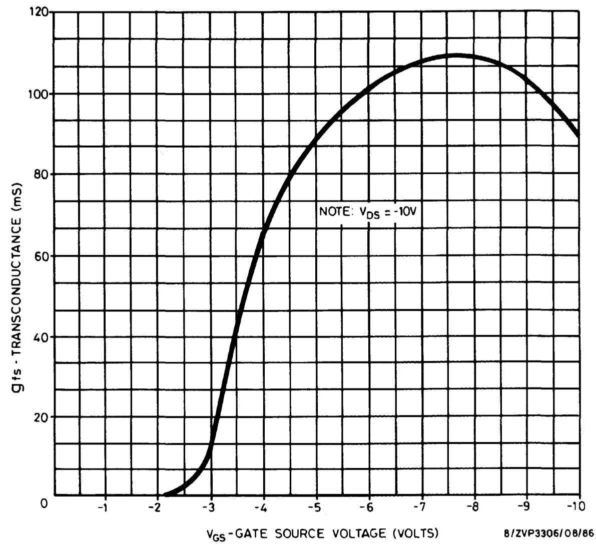


Fig. 8 Typical transconductance v gate-source voltage

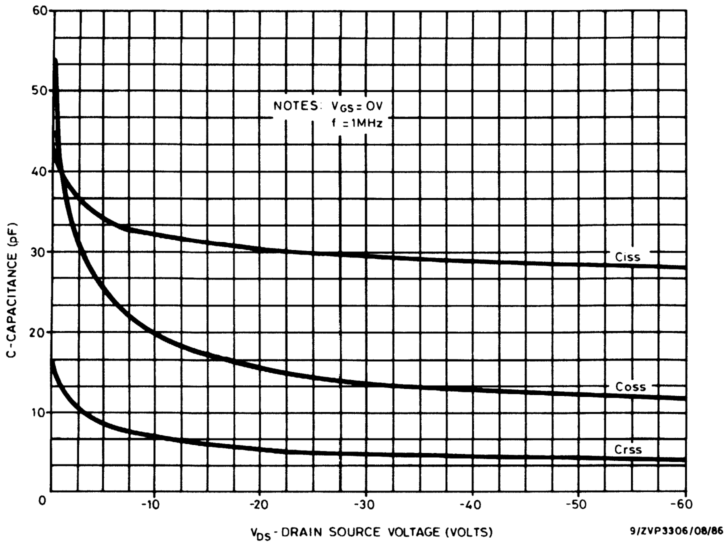


Fig. 9 Typical capacitance v drain-source voltage

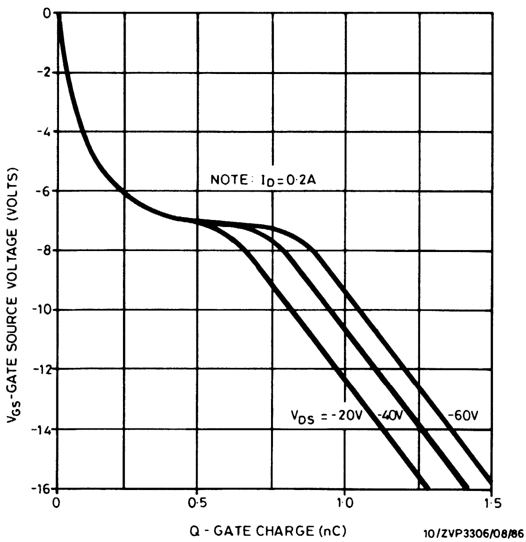


Fig. 10 Typical gate charge v gate-source voltage

BS250F

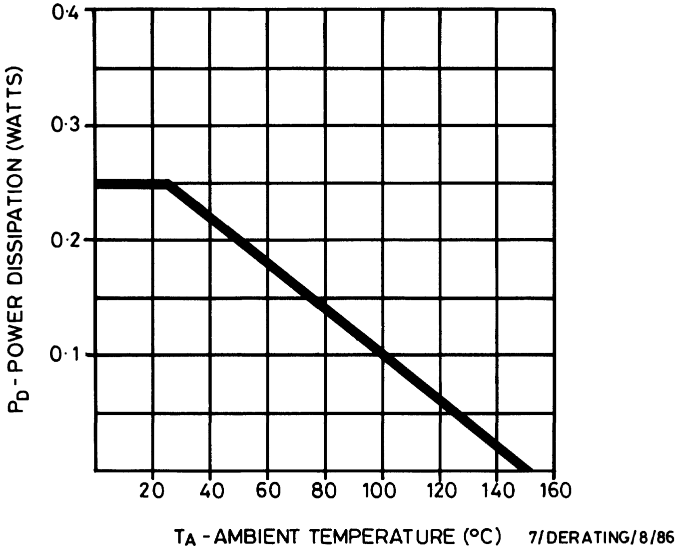


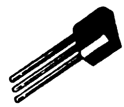
Fig. 11 Power v temperature derating curve (ambient)

P-channel enhancement mode vertical DMOS FET

BS250P

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
BS250P	−45V	−0.23A	14Ω

BS250P

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	−45	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.23	A
I_{DM}	Pulse drain current	−3	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−45	−70	–	V	$I_D = -100\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1	–	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	−20	nA	$V_{GS} = -15V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	−0.5	μA	$V_{DS} = -25V$, $V_{GS} = 0V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	14	Ω	$I_D = -200mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	–	150	–	mS	$V_{DS} = -10V$, $I_D = -200mA$
C_{iss}	Input capacitance (2)	–	60	–	pF	$V_{DS} = -10V$, $V_{GS} = 0V$ f = 1MHz
$t_{d(on)}$	Turn-on delay time (2) (3)	–	–	10	ns	$V_{DD} \approx -25V$, $I_D = -500mA$
t_r	Rise time (2) (3)	–	–	12	ns	$V_{DD} \approx -25V$, $I_D = -500mA$
$t_{d(off)}$	Turn-off delay time (2) (3)	–	–	10	ns	$V_{DD} \approx -25V$, $I_D = -500mA$
t_f	Fall time (2) (3)	–	–	10	ns	$V_{DD} \approx -25V$, $I_D = -500mA$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

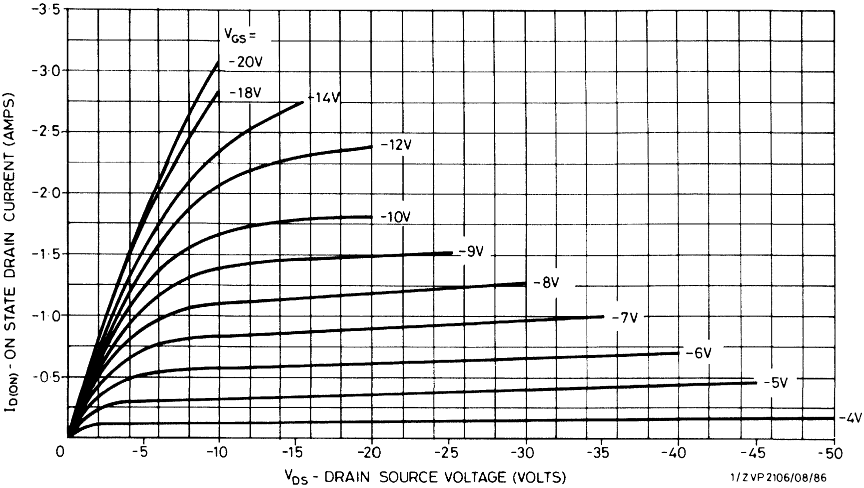


Fig. 1 Typical output characteristics

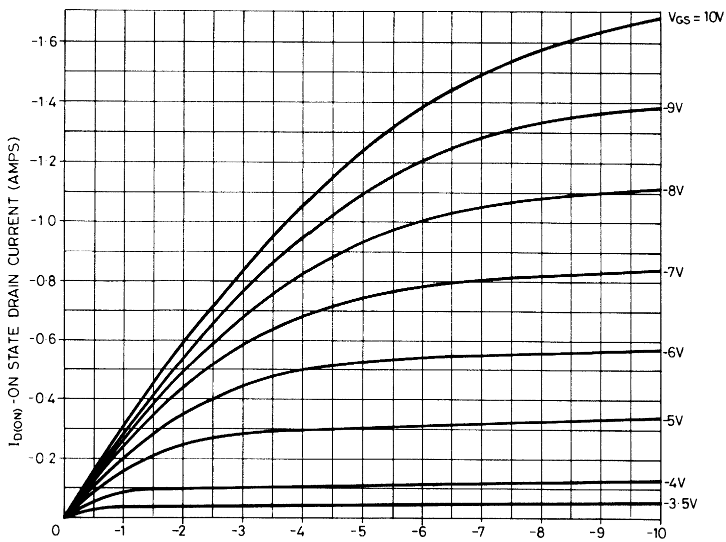


Fig. 2 Typical saturation characteristics

BS250P

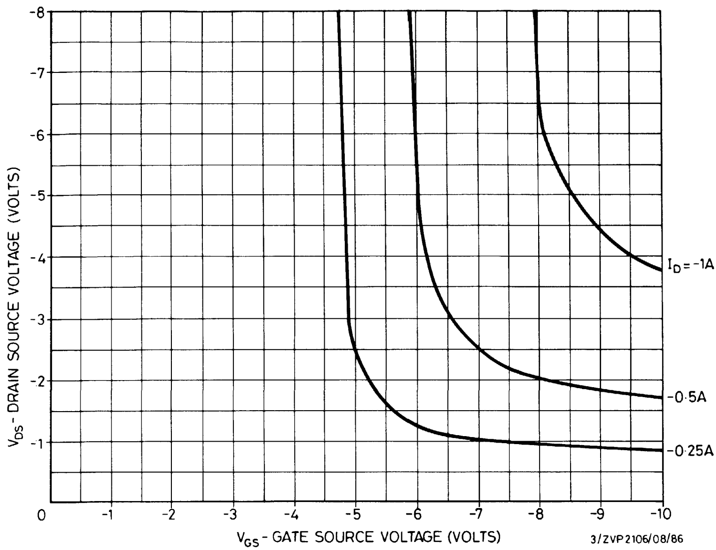


Fig. 3 Typical voltage saturation characteristics

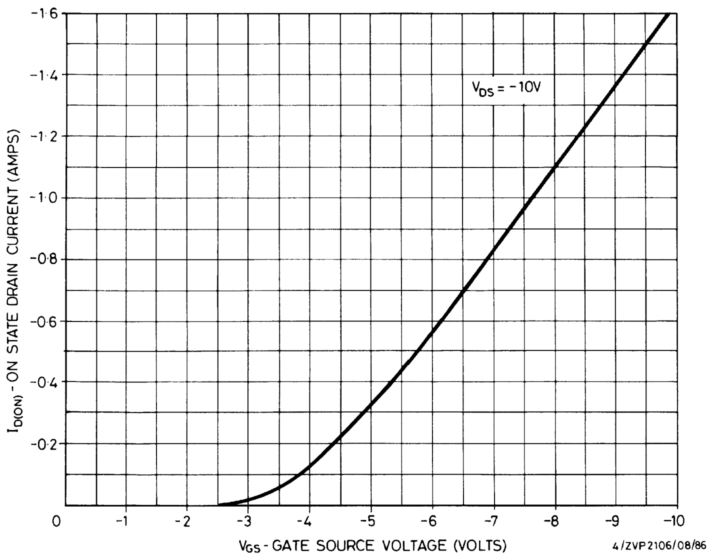


Fig. 4 Typical transfer characteristics

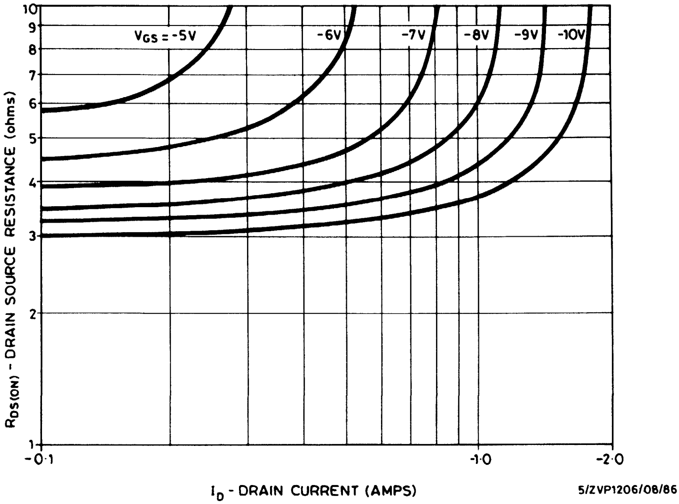


Fig. 5 Typical on-resistance v drain current

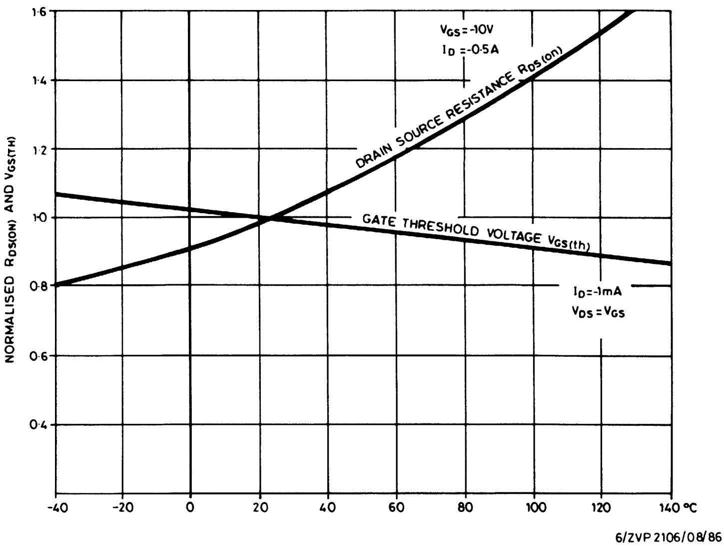


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

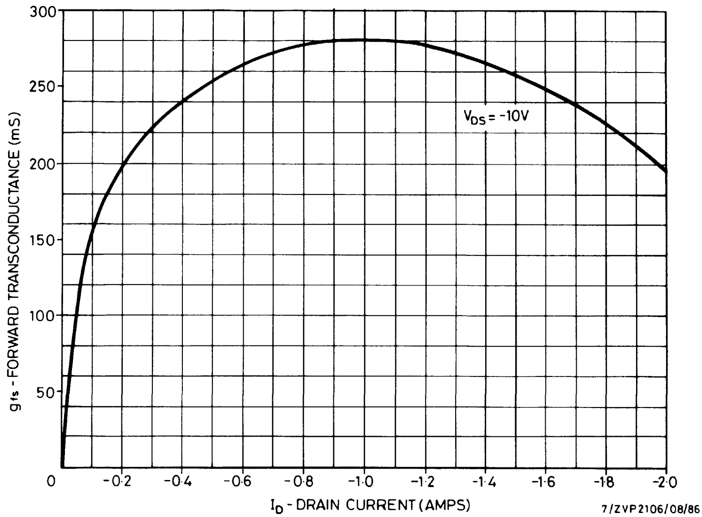


Fig. 7 Typical transconductance v drain current

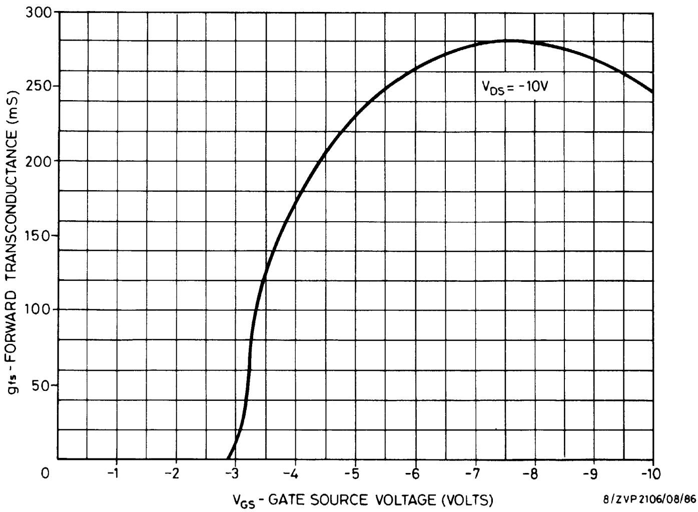


Fig. 8 Typical transconductance v gate-source voltage

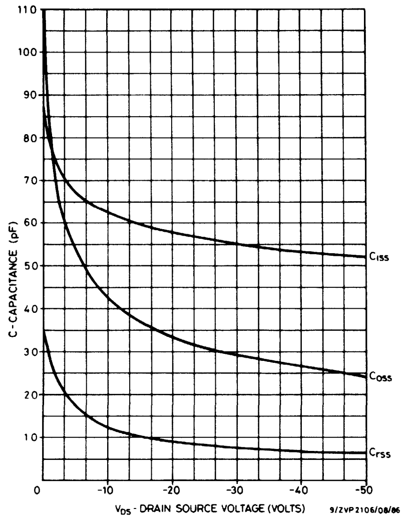


Fig. 9 Typical capacitance v drain-source voltage

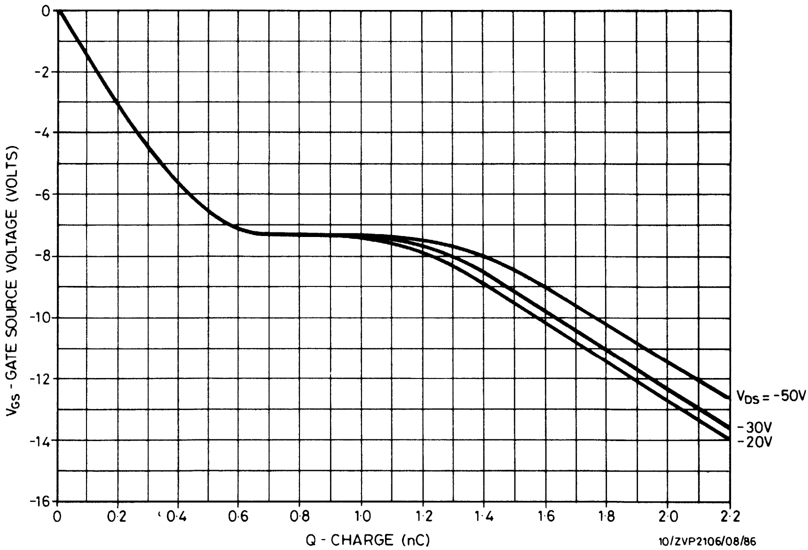


Fig. 10 Typical gate charge v gate-source voltage

BS250P

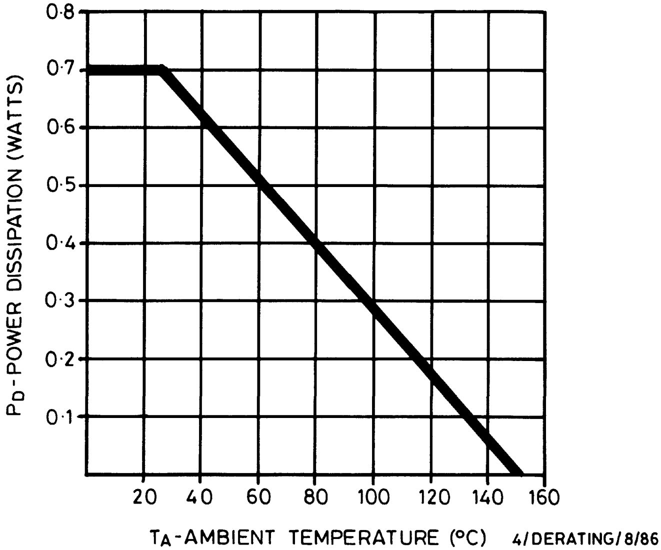


Fig. 11 Power v temperature derating curve (ambient)

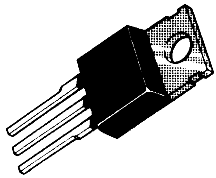
N-channel enhancement mode vertical DMOS FET

IRFZ20 IRFZ22

ADVANCED INFORMATION

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-220

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
IRFZ20	50V	15A	0.10Ω
IRFZ22	50V	14A	0.12Ω

IRFZ20 IRFZ22

ABSOLUTE MAXIMUM RATINGS

	Parameter	IRFZ20	IRFZ22	Units
V_{DS}	Drain-source voltage	50	50	V
I_D	Continuous drain current (@ $T_C = 25°C$)	15	14	A
I_{DM}	Pulse drain current	60	56	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_C = 25°C$)	40	40	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Part No.	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	IRFZ20 IRFZ22	50	–	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$V_{GS(th)}$	Gate threshold voltage	All	2	4	V	$V_{GS} = V_{DS}$, $I_D = 250\mu A$
I_{GSS}	Gate-body leakage	All	–	500	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	All	–	250	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		All	–	1000	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	IRFZ20	15	–	A	$V_{DS} = 10V$, $V_{GS} = 10V$
		IRFZ22	14	–	A	
$R_{DS(on)}$	Static drain-source on-state resistance (1)	IRFZ20	–	0.1	Ω	$I_D = 9A$, $V_{GS} = 10V$
		IRFZ22	–	0.12	Ω	
g_{fs}	Forward transconductance (1) (2)	All	5	–	S	$V_{DS} = 10V$, $I_D = 9A$
C_{iss}	Input capacitance (2)	All	–	850	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	All	–	350	pF	
C_{rss}	Reverse transfer capacitance (2)	All	–	100	pF	
$t_{d(on)}$	Turn-on delay time (2)	All	–	30	ns	$V_{DD} \approx 25V$, $I_D = 9A$ $Z_O = 50\Omega$
t_r	Rise time (2)	All	–	90	ns	
$t_{d(off)}$	Turn-off delay time (2)	All	–	40	ns	
t_f	Fall time (2)	All	–	30	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

Parameter	Part No.	Typ.	Max.	Unit	Conditions
V_{SD} Diode forward voltage (1)	IRFZ20	–	1.25	V	$V_{GS} = 0V$, $I_S = 15A$ $T_C = 25°C$
	IRFZ22	–	1.10	V	$V_{GS} = 0V$, $I_S = 14A$ $T_C = 25°C$
t_{rr} Reverse recovery time (2)	All	100	–	ns	$I_F = 15A$, $dI_F/dt = 100A/\mu s$ $T_j = 150°C$

(1) Measured under pulsed conditions. Width $= 300\mu s$. Duty cycle $\leqslant 2\%$.
(2) Sample test.

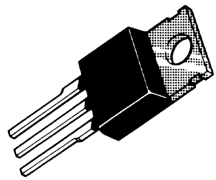
N-channel enhancement mode vertical DMOS FET

IRFZ30 IRFZ32

ADVANCED INFORMATION

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-220

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
IRFZ30	50V	30A	0.05Ω
IRFZ32	50V	25A	0.07Ω

ABSOLUTE MAXIMUM RATINGS

	Parameter	IRFZ30	IRFZ32	Units
V_{DS}	Drain-source voltage	50	50	V
I_D	Continuous drain current (@ $T_C = 25°C$)	30	25	A
I_{DM}	Pulse drain current	80	60	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_C = 25°C$)	75	75	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Part No.	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	IRFZ30 IRFZ32	50	–	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$V_{GS(th)}$	Gate threshold voltage	All	2	4	V	$V_{GS} = V_{DS}$, $I_D = 250\mu A$
I_{GSS}	Gate-body leakage	All	–	500	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	All	–	250	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		All	–	1000	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	IRFZ30	30	–	A	$V_{DS} = 10V$, $V_{GS} = 10V$
		IRFZ32	25	–	A	
$R_{DS(on)}$	Static drain-source on-state resistance (1)	IRFZ30	–	0.05	Ω	$I_D = 16A$, $V_{GS} = 10V$
		IRFZ32	–	0.07	Ω	
g_{fs}	Forward transconductance (1) (2)	All	9	–	S	$V_{DS} = 10V$, $I_D = 16A$
C_{iss}	Input capacitance (2)	All	–	1600	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	All	–	800	pF	
C_{rss}	Reverse transfer capacitance (2)	All	–	200	pF	
$t_{d(on)}$	Turn-on delay time (2)	All	–	25	ns	$V_{DD} \approx 25V$, $I_D = 16A$ $Z_O = 50\Omega$
t_r	Rise time (2)	All	–	35	ns	
$t_{d(off)}$	Turn-off delay time (2)	All	–	45	ns	
t_f	Fall time (2)	All	–	35	ns	

IRFZ30 IRFZ32

SOURCE-DRAIN DIODE CHARACTERISTICS

Parameter	Part No.	Typ.	Max.	Unit	Conditions
V_{SD} Diode forward voltage (1)	IRFZ30	–	1.6	V	$V_{GS} = 0V$, $I_S = 30A$ $T_C = 25°C$
	IRFZ32	–	1.5	V	$V_{GS} = 0V$, $I_S = 25A$ $T_C = 25°C$
t_{rr} Reverse recovery time (2)	All	160	–	ns	$I_F = 30A$, $dI_F/dt = 100A/\mu s$ $T_j = 150°C$

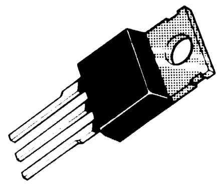
(1) Measured under pulsed conditions. Width = 300μs. Duty cycle $\leqslant$ 2%.
(2) Sample test.

N-channel enhancement mode vertical DMOS FET

IRF520 IRF521 IRF522 IRF523

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-220

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
IRF520	100V	8A	0.3Ω
IRF521	60V	8A	0.3Ω
IRF522	100V	7A	0.4Ω
IRF523	60V	7A	0.4Ω

IRF520 IRF521 IRF522 IRF523

ABSOLUTE MAXIMUM RATINGS

	Parameter	IRF520	IRF521	IRF522	IRF523	Units
V_{DS}	Drain-source voltage	100	60	100	60	V
I_D	Continuous drain current (@ $T_C = 25°C$)	8	8	7	7	A
I_{DM}	Pulse drain current	32	32	28	28	A
V_{GS}	Gate-source voltage	±20	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_C = 25°C$)	40	40	40	40	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150				°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Part No.	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	IRF520 IRF522	100	–	V	$V_{GS} = 0V$, $I_D = 250\mu A$
		IRF521 IRF523	60	–	V	
$V_{GS(th)}$	Gate threshold voltage	All	2	4	V	$V_{GS} = V_{DS}$, $I_D = 250\mu A$
I_{GSS}	Gate-body leakage	All	–	500	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	All	–	250	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		All	–	1000	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	IRF520 IRF521	8	–	A	$V_{DS} = 5V$, $V_{GS} = 10V$
		IRF522 IRF523	7	–	A	
$R_{DS(on)}$	Static drain-source on-state resistance (1)	IRF520 IRF521	–	0.3	Ω	$I_D = 4A$, $V_{GS} = 10V$
		IRF522 IRF523	–	0.4	Ω	
g_{fs}	Forward transconductance (1) (2)	All	1.5	–	S	$V_{DS} = 5V$, $I_D = 4A$

ELECTRICAL CHARACTERISTICS cont.

Parameter		Part No.	Min.	Max.	Unit	Conditions
C_{iss}	Input capacitance (2)	All	–	600	pF	$V_{DS}=25V$, $V_{GS}=0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	All	–	400	pF	
C_{rss}	Reverse transfer capacitance (2)	All	–	100	pF	
$t_{d(on)}$	Turn-on delay time (2)	All	–	40	ns	$V_{DD}\approx 36V$, $I_D=4A$ $Z_O=50\Omega$
t_r	Rise time (2)	All	–	70	ns	
$t_{d(off)}$	Turn-off delay time (2)	All	–	100	ns	
t_f	Fall time (2)	All	–	70	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

Parameter		Part No.	Typ.	Max.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	IRF520 IRF521	–	2.5	V	$V_{GS}=0V$, $I_S=8A$ $T_C=25°C$
		IRF522 IRF523	–	2.3	V	$V_{GS}=0V$, $I_S=7A$ $T_C=25°C$
t_{rr}	Reverse recovery time (2)	All	280	–	ns	$I_F=8A$, $dI_F/dt=100A/\mu s$ $T_j=150°C$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.

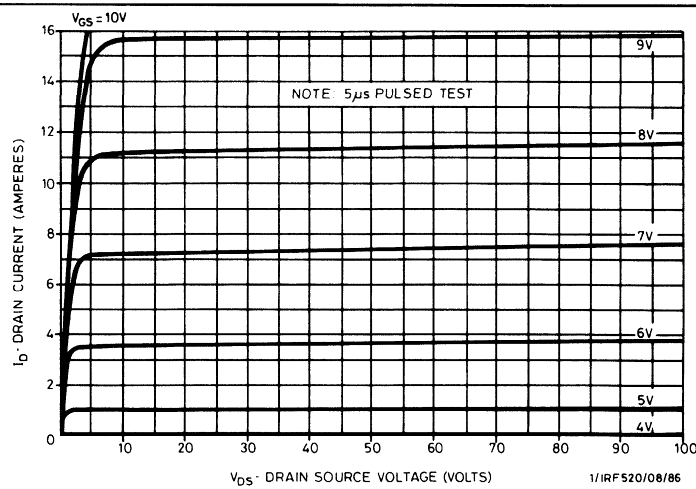


Fig. 1 Typical output characteristics

IRF520 IRF521 IRF522 IRF523

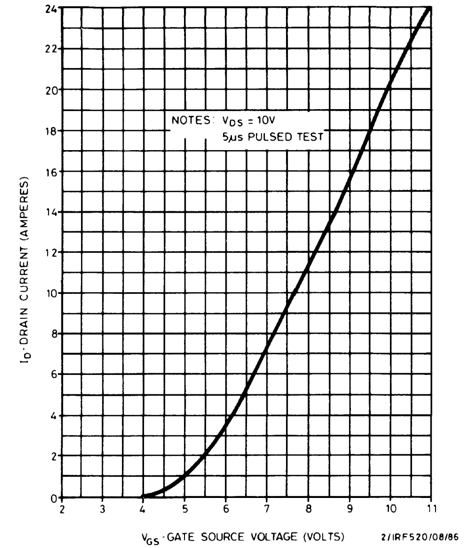


Fig. 2 Typical transfer characteristics

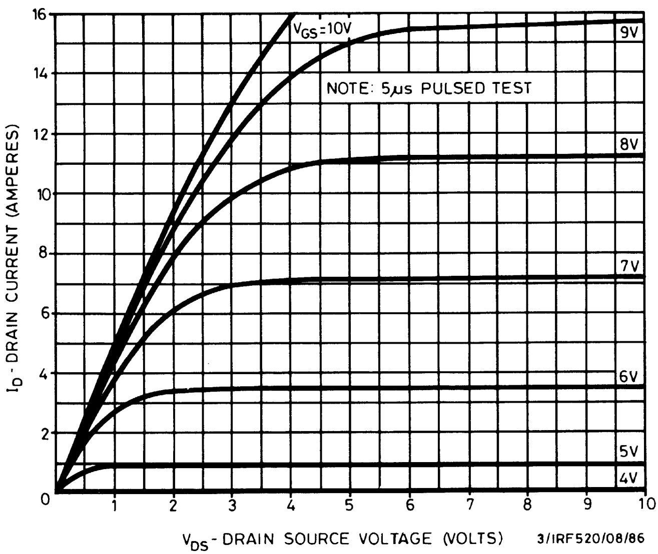


Fig. 3 Typical saturation characteristics

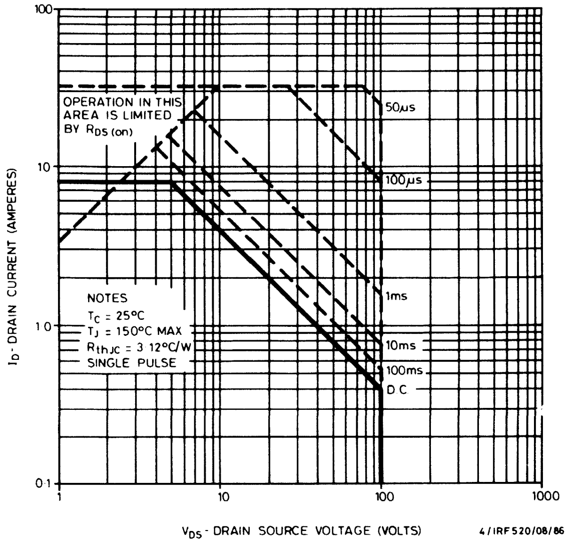


Fig. 4 Maximum safe operating area

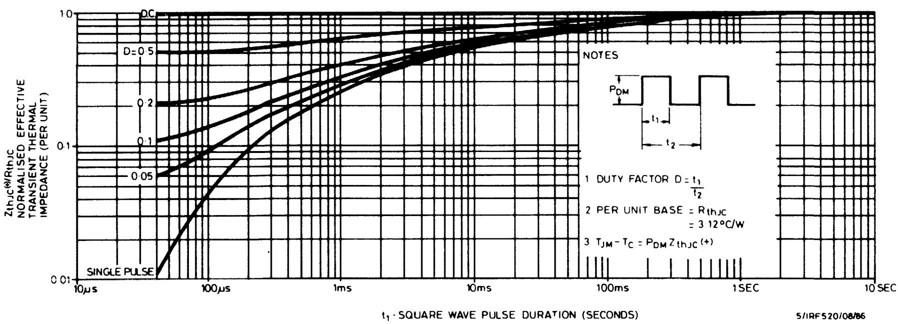


Fig. 5 Maximum effective transient thermal impedance, junction-case v pulse duration

IRF520 IRF521 IRF522 IRF523

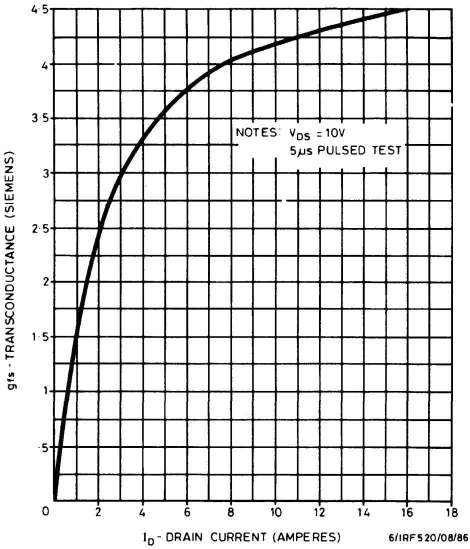


Fig. 6 Typical transconductance v drain current

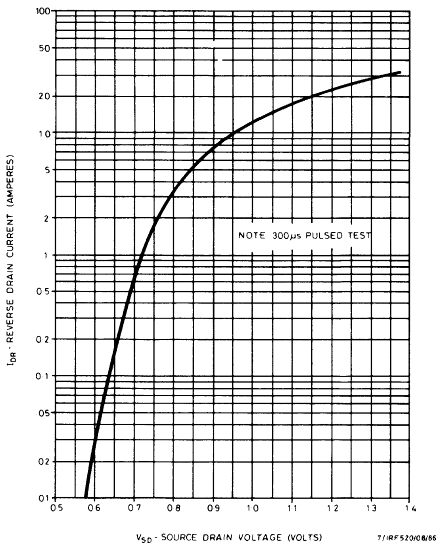


Fig. 7 Typical source-drain diode forward voltage

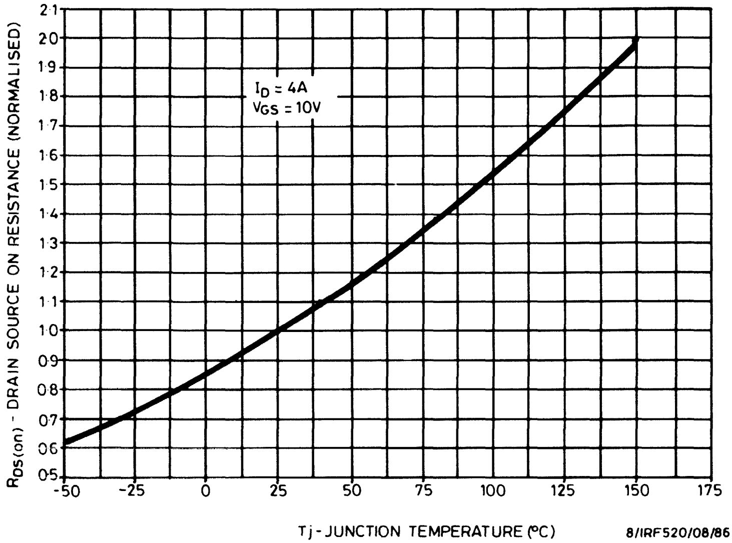


Fig. 8 Normalised on-resistance v temperature

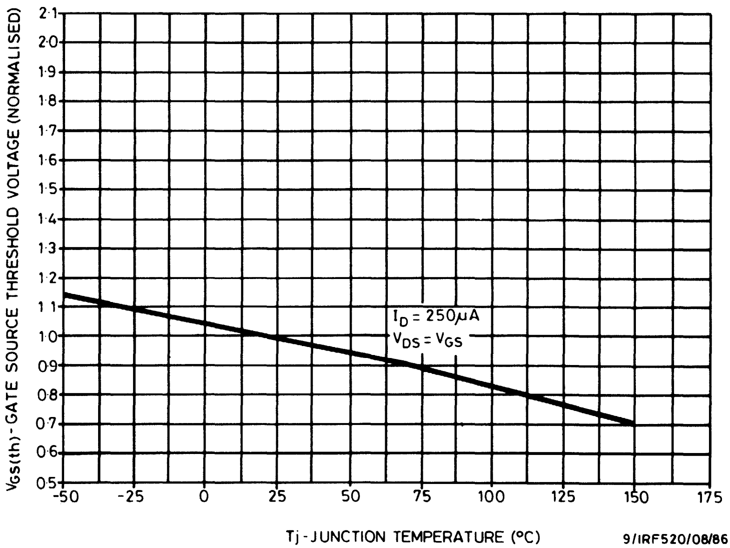


Fig. 9 Normalised gate threshold voltage v temperature

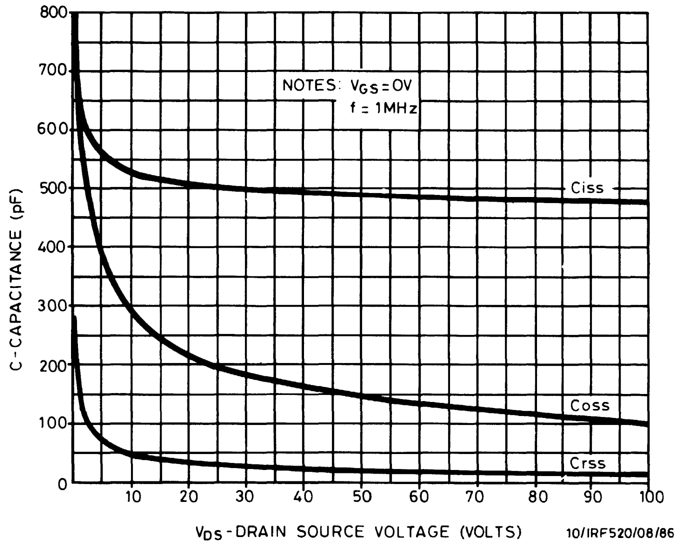


Fig. 10 Typical capacitance v drain-source voltage

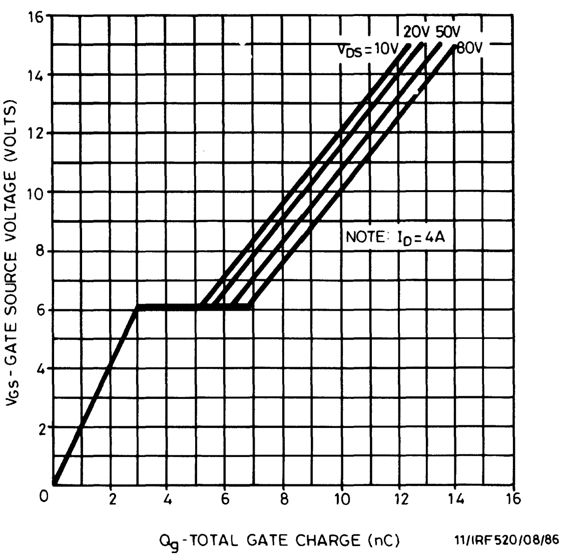


Fig. 11 Typical gate charge v gate-source voltage

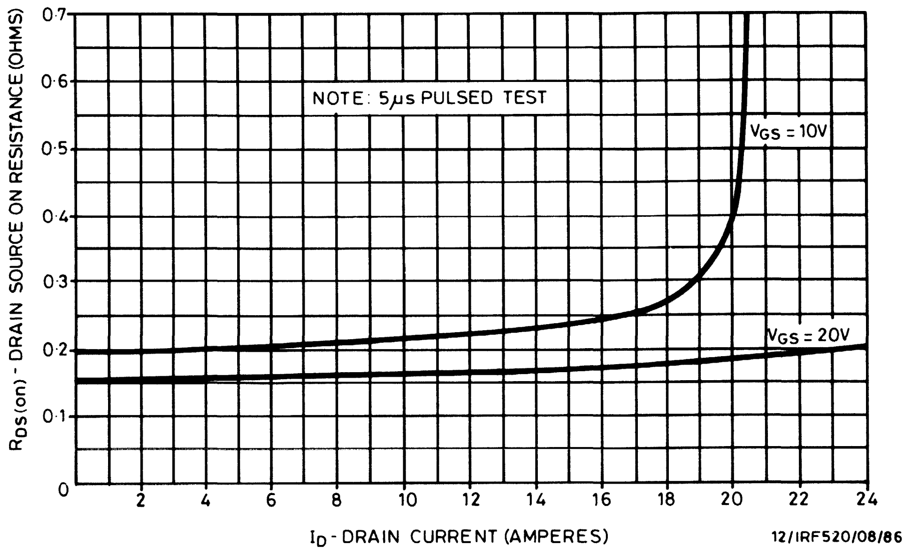


Fig. 12 Typical on-resistance v drain current

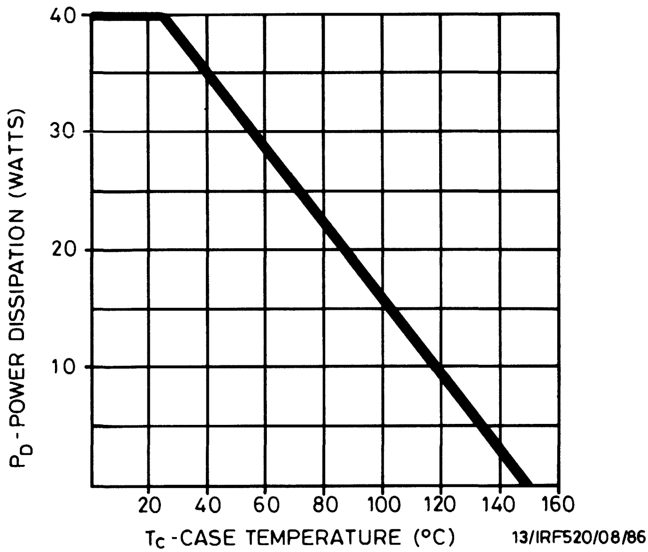
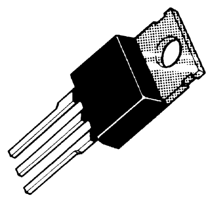


Fig. 13 Power v temperature derating curve

N-channel enhancement mode vertical DMOS FET

IRF530 IRF531 IRF532 IRF533



TO-220

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
IRF530	100V	14A	0.18Ω
IRF531	60V	14A	0.18Ω
IRF532	100V	12A	0.25Ω
IRF533	60V	12A	0.25Ω

ABSOLUTE MAXIMUM RATINGS

	Parameter	IRF530	IRF531	IRF532	IRF533	Units
V_{DS}	Drain-source voltage	100	60	100	60	V
I_D	Continuous drain current (@ $T_C = 25°C$)	14	14	12	12	A
I_{DM}	Pulse drain current	56	56	48	48	A
V_{GS}	Gate-source voltage	±20	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_C = 25°C$)	75	75	75	75	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150				°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Part No.	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	IRF530 IRF532	100	–	V	$V_{GS} = 0V$, $I_D = 250\mu A$
		IRF531 IRF533	60	–	V	
$V_{GS(th)}$	Gate threshold voltage	All	2	4	V	$V_{GS} = V_{DS}$, $I_D = 250\mu A$
I_{GSS}	Gate-body leakage	All	–	500	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	All	–	250	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		All	–	1000	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	IRF530 IRF531	14	–	A	$V_{DS} = 10V$, $V_{GS} = 10V$
		IRF532 IRF533	12	–	A	
$R_{DS(on)}$	Static drain-source on-state resistance (1)	IRF530 IRF531	–	0.18	Ω	$I_D = 8A$, $V_{GS} = 10V$
		IRF532 IRF533	–	0.25	Ω	
g_{fs}	Forward transconductance (1) (2)	All	4	–	S	$V_{DS} = 10V$, $I_D = 8A$

ELECTRICAL CHARACTERISTICS cont.

Parameter		Part No.	Min.	Max.	Unit	Conditions
C_{iss}	Input capacitance (2)	All	–	800	pF	$V_{DS}=25V$, $V_{GS}=0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	All	–	500	pF	
C_{rss}	Reverse transfer capacitance (2)	All	–	150	pF	
$t_{d(on)}$	Turn-on delay time (2)	All	–	30	ns	$V_{DD}\approx 36V$, $I_D=8A$ $Z_O=15\Omega$
t_r	Rise time (2)	All	–	75	ns	
$t_{d(off)}$	Turn-off delay time (2)	All	–	40	ns	
t_f	Fall time (2)	All	–	45	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

Parameter		Part No.	Typ.	Max.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	IRF530 IRF531	–	2.5	V	$V_{GS}=0V$, $I_S=14A$ $T_C=25°C$
		IRF532 IRF533	–	2.3	V	$V_{GS}=0V$, $I_S=12A$ $T_C=25°C$
t_{rr}	Reverse recovery time (2)	All	360	–	ns	$I_F=14A$, $dI_F/dt=100A/\mu s$ $T_j=150°C$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤2%.
(2) Sample test.

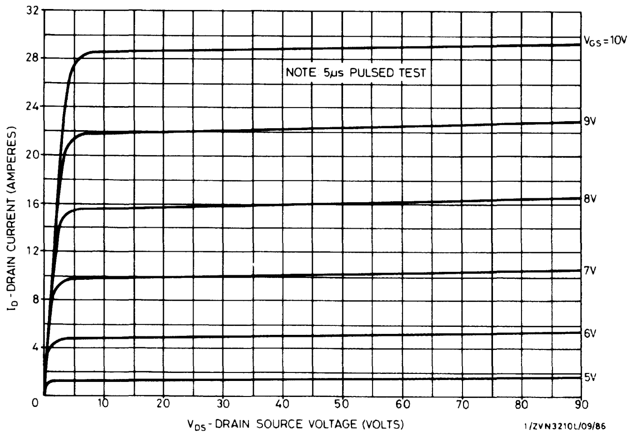


Fig. 1 Typical output characteristics

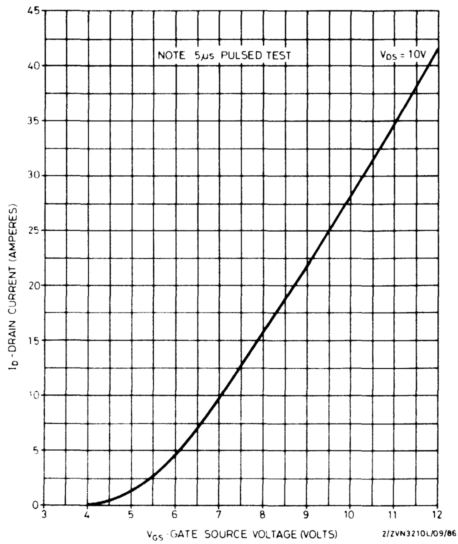


Fig. 2 Typical transfer characteristics

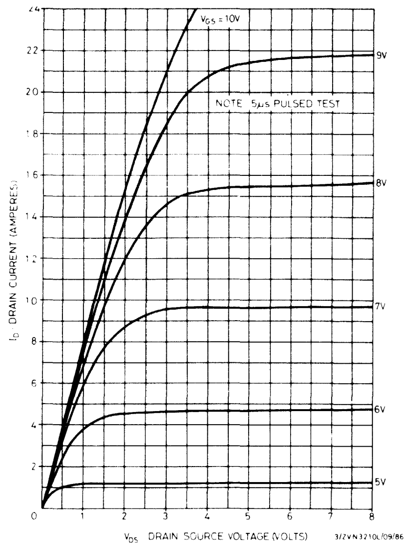


Fig. 3 Typical saturation characteristics

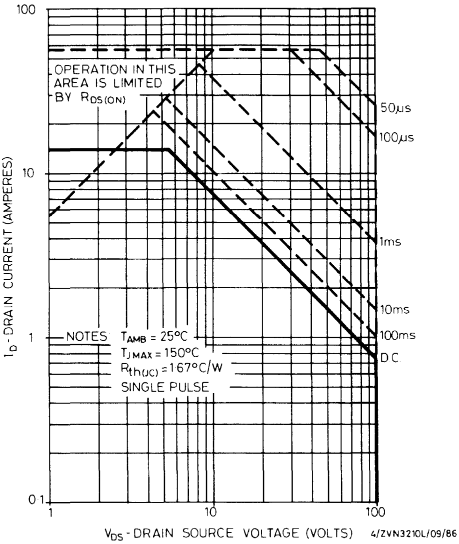


Fig. 4 Maximum safe operating area

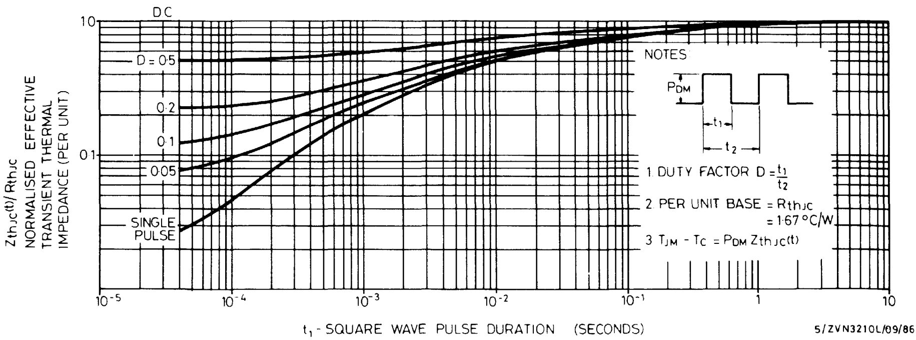


Fig. 5 Maximum effective transient thermal impedance, junction-case v pulse duration

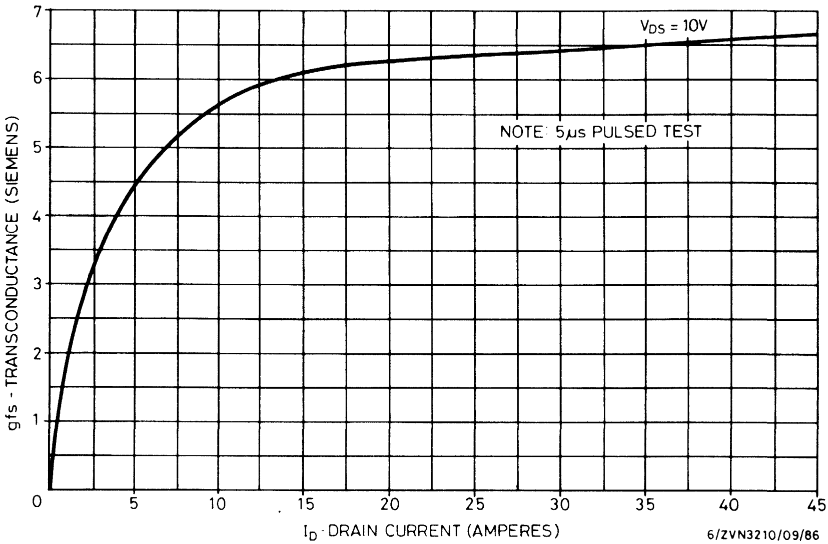


Fig. 6 Typical transconductance v drain current

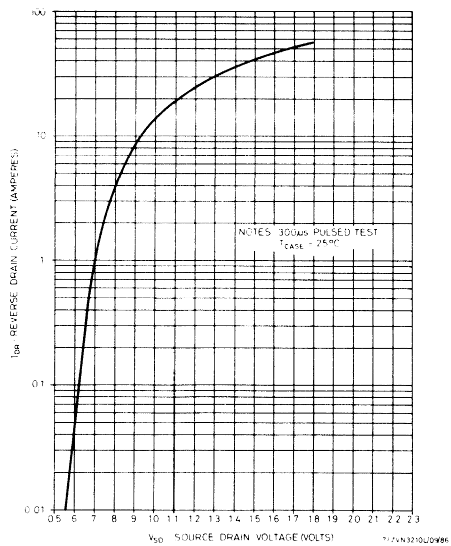


Fig. 7 Typical source-drain diode forward voltage

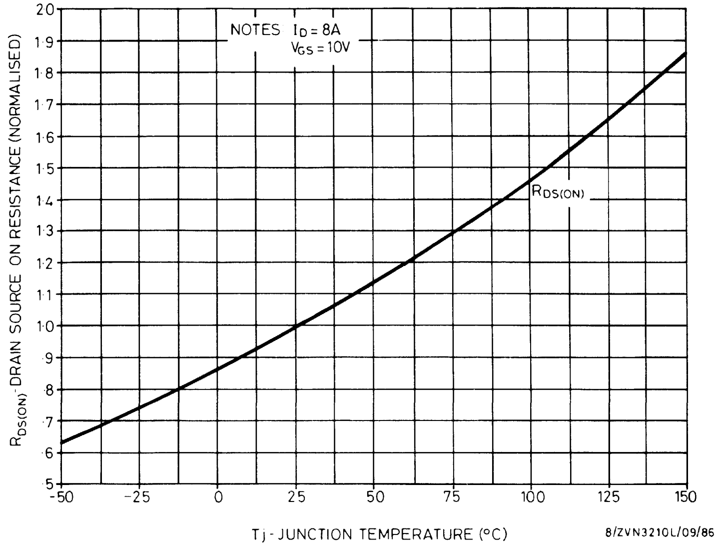


Fig. 8 Normalised on-resistance v temperature

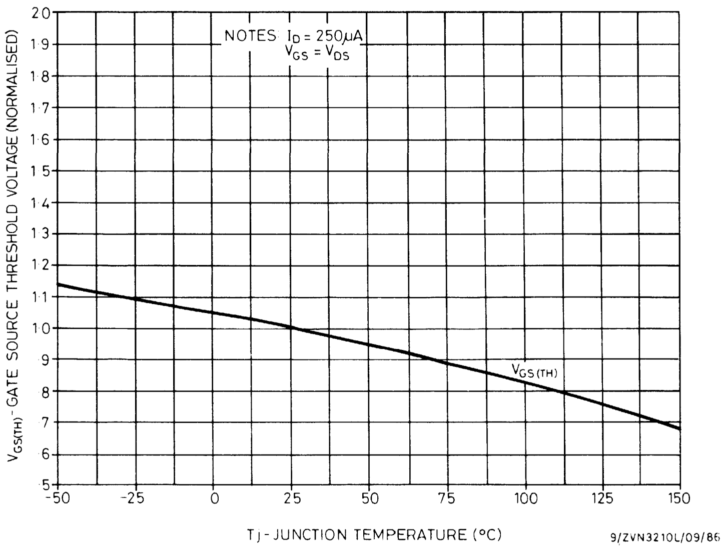


Fig. 9 Normalised gate threshold voltage v temperature

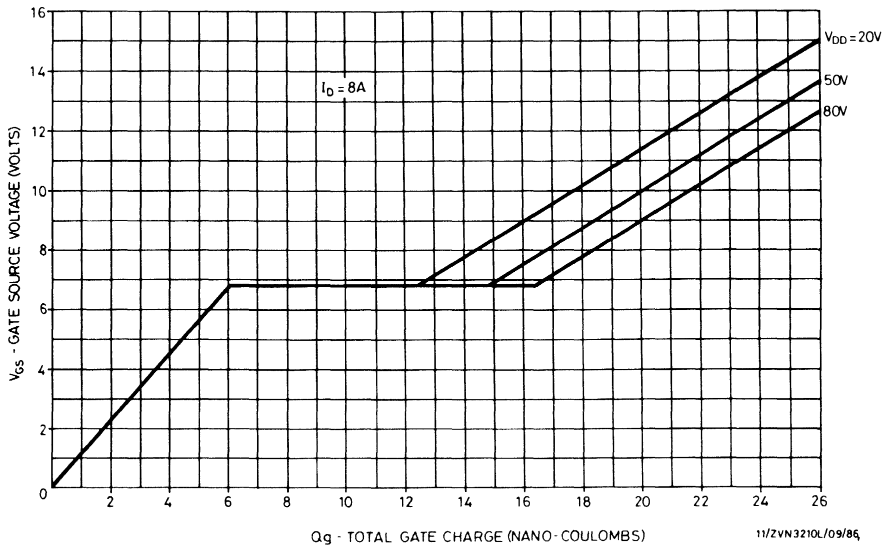


Fig. 10 Typical gate charge v gate-source voltage

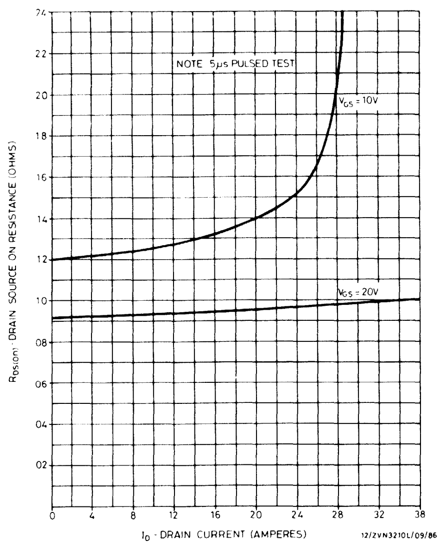


Fig. 11 Typical on-resistance v drain current

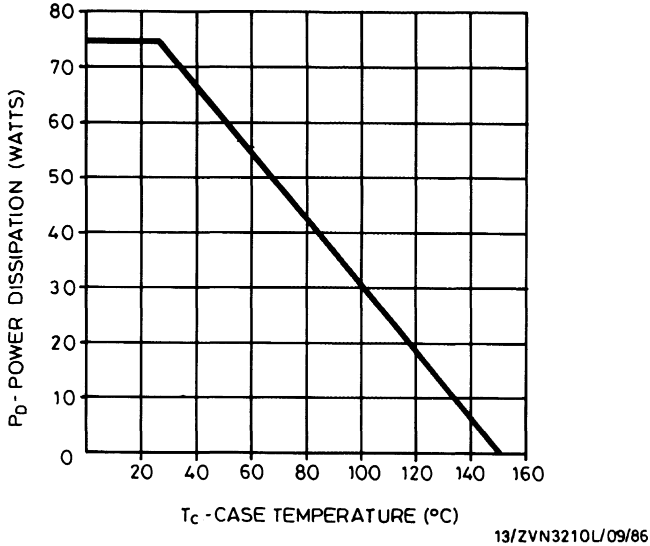


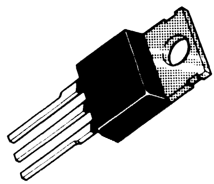
Fig. 12 Power v temperature derating curve

N-channel enhancement mode vertical DMOS FET

IRF620 IRF621 IRF622 IRF623

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-220

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
IRF620	200V	5A	0.8Ω
IRF621	150V	5A	0.8Ω
IRF622	200V	4A	1.2Ω
IRF623	150V	4A	1.2Ω

IRF620 IRF621 IRF622 IRF623

ABSOLUTE MAXIMUM RATINGS

	Parameter	IRF620	IRF621	IRF622	IRF623	Units
V_{DS}	Drain-source voltage	200	150	200	150	V
I_D	Continuous drain current (@ $T_C = 25°C$)	5	5	4	4	A
I_{DM}	Pulse drain current	20	20	16	16	A
V_{GS}	Gate-source voltage	±20	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_C = 25°C$)	40	40	40	40	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150				°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Part No.	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	IRF620 IRF622	200	–	V	$V_{GS} = 0V$, $I_D = 250\mu A$
		IRF621 IRF623	150	–	V	
$V_{GS(th)}$	Gate threshold voltage	All	2	4	V	$V_{GS} = V_{DS}$, $I_D = 250\mu A$
I_{GSS}	Gate body leakage	All	–	500	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	All	–	250	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		All	–	1000	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	IRF620 IRF621	5	–	A	$V_{DS} = 10V$, $V_{GS} = 10V$
		IRF622 IRF623	4	–	A	
$R_{DS(on)}$	Static drain-source on-state resistance (1)	IRF620 IRF621	–	0.8	Ω	$I_D = 2.5A$, $V_{GS} = 10V$
		IRF622 IRF623	–	1.2	Ω	
g_{fs}	Forward transconductance (1) (2)	All	1.3	–	S	$V_{DS} = 10V$, $I_D = 2.5A$

ELECTRICAL CHARACTERISTICS cont.

Parameter		Part No.	Min.	Max.	Unit	Conditions
C_{iss}	Input capacitance (2)	All	–	600	pF	$V_{DS}=25V$, $V_{GS}=0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	All	–	300	pF	
C_{rss}	Reverse transfer capacitance (2)	All	–	80	pF	
$t_{d(on)}$	Turn-on delay time (2)	All	–	40	ns	$V_{DD}\approx 90V$, $I_D=2.5A$ $Z_O=50\Omega$
t_r	Rise time (2)	All	–	60	ns	
$t_{d(off)}$	Turn-off delay time (2)	All	–	100	ns	
t_f	Fall time (2)	All	–	60	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

Parameter		Part No.	Typ.	Max.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	IRF620 IRF621	–	1.8	V	$V_{GS}=0V$, $I_S=5A$ $T_C=25°C$
		IRF622 IRF623	–	1.4	V	$V_{GS}=0V$, $I_S=4A$ $T_C=25°C$
t_{rr}	Reverse recovery time (2)	All	350	–	ns	$I_F=5A$, $dI_F/dt=100A/\mu s$ $T_j=150°C$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤2%.
(2) Sample test.

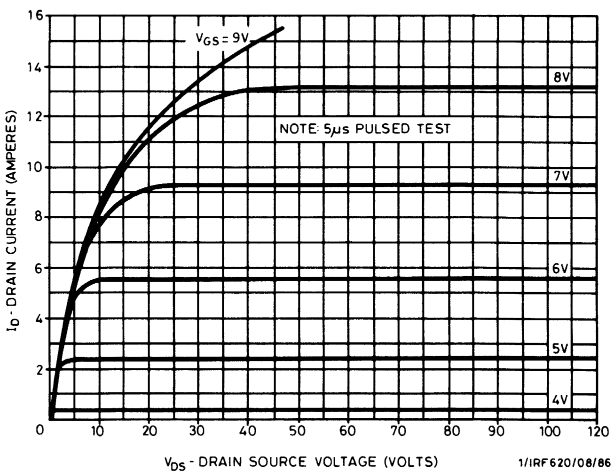


Fig. 1 Typical output characteristics

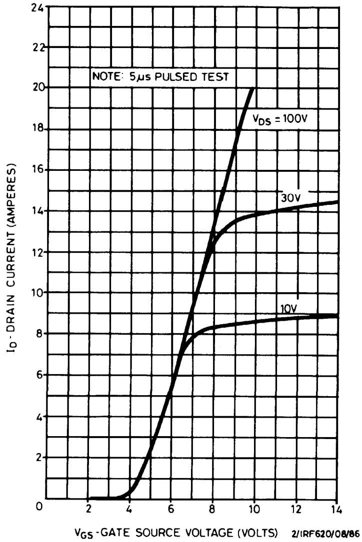


Fig. 2 Typical transfer characteristics

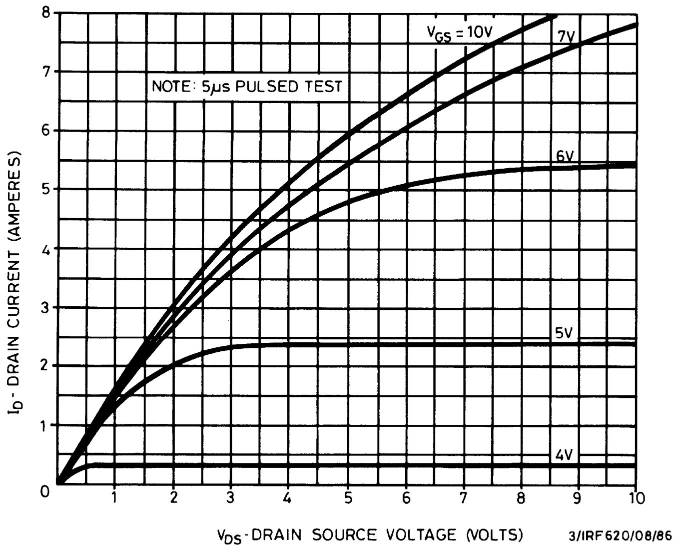


Fig. 3 Typical saturation characteristics

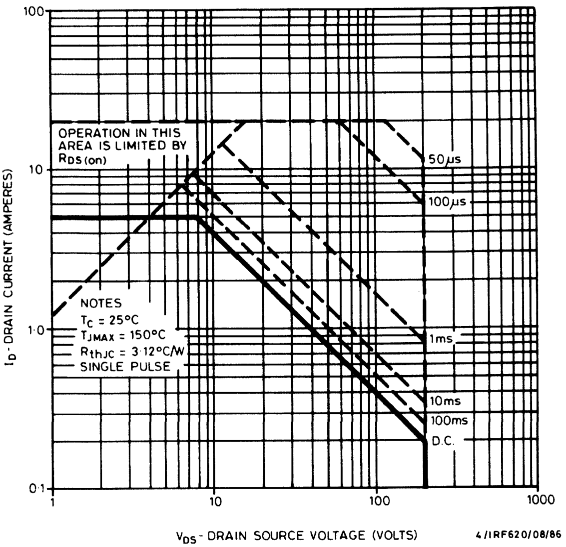


Fig. 4 Maximum safe operating area

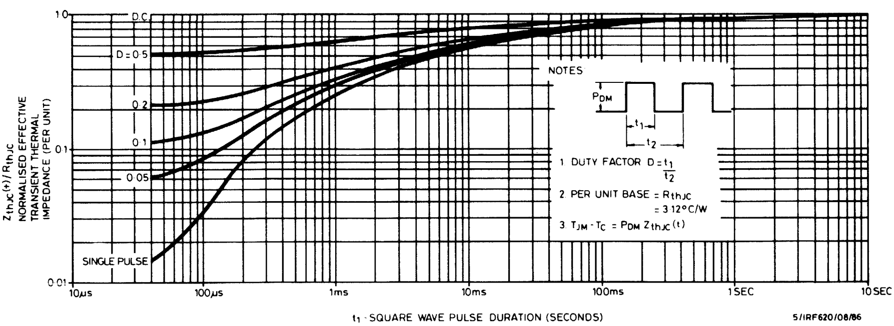


Fig. 5 Maximum effective transient thermal impedance, junction-case v pulse duration

IRF620 IRF621 IRF622 IRF623

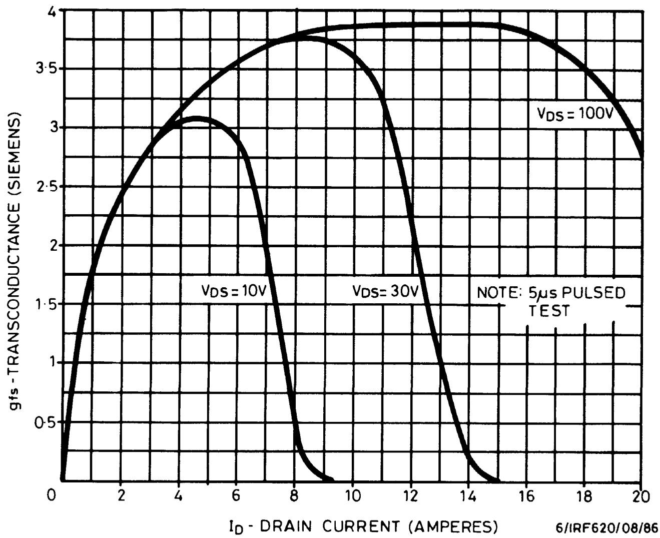


Fig. 6 Typical transconductance v drain current

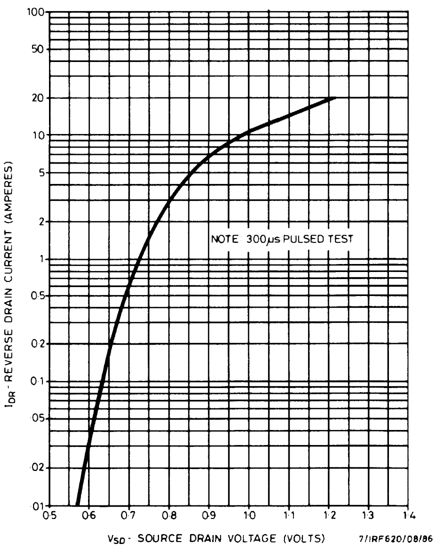


Fig. 7 Typical source-drain diode forward voltage

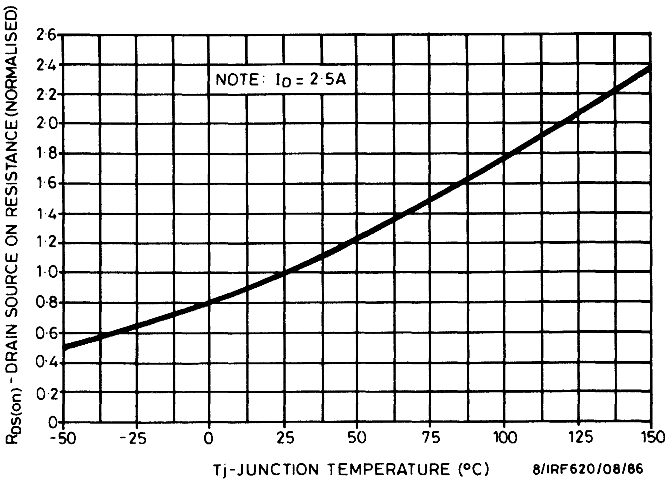


Fig. 8 Normalised on-resistance v temperature

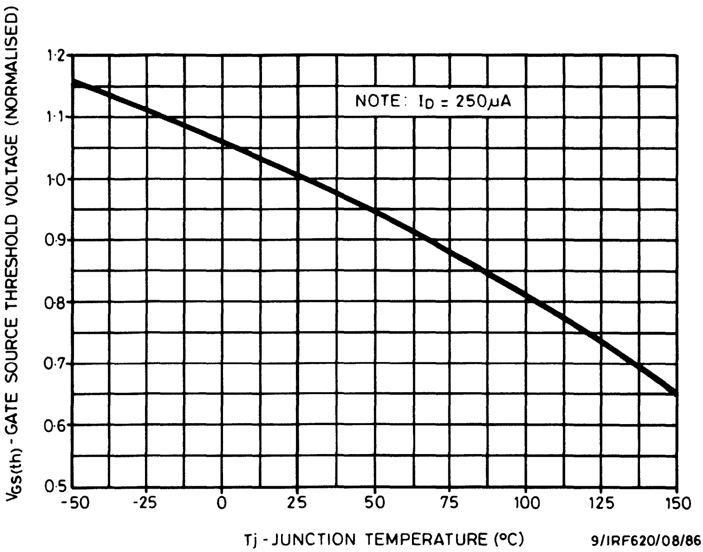


Fig. 9 Normalised gate threshold voltage v temperature

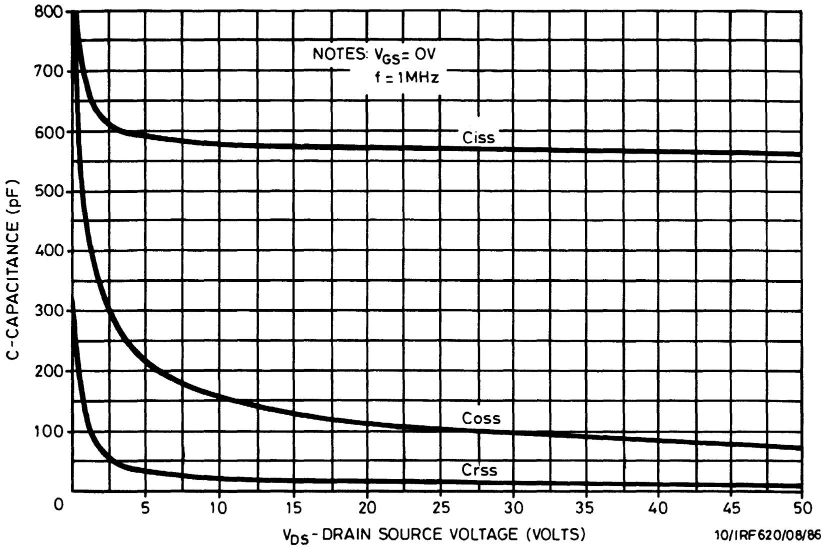


Fig. 10 Typical capacitance v drain-source voltage

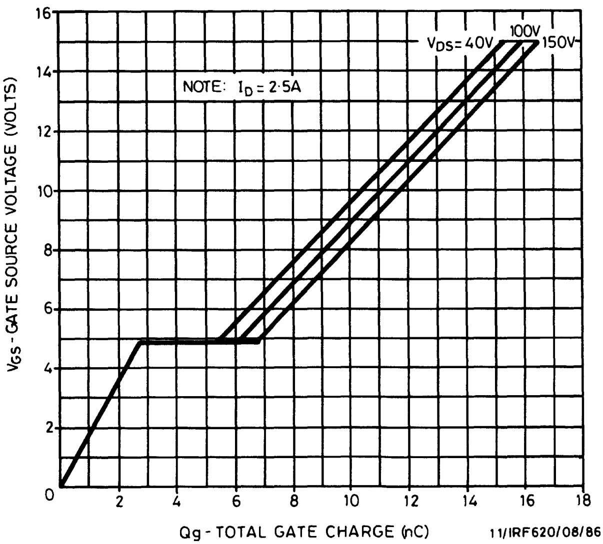


Fig. 11 Typical gate charge v gate-source voltage

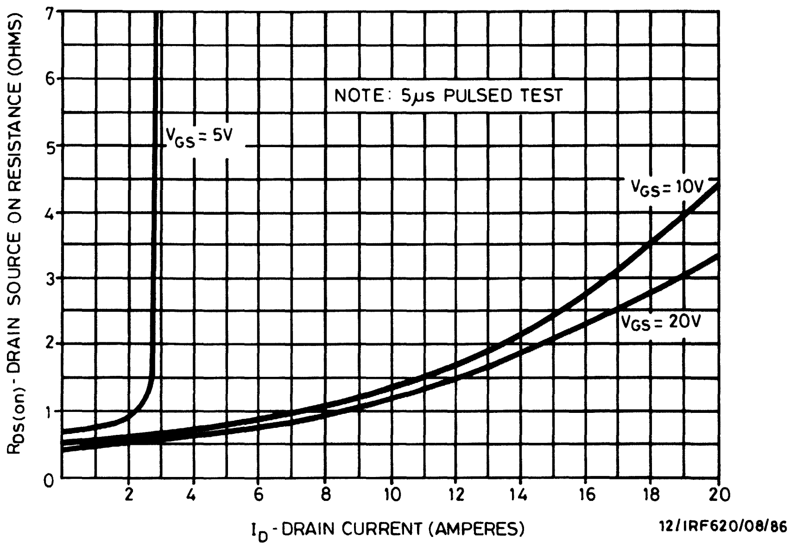


Fig. 12 Typical on-resistance v drain current

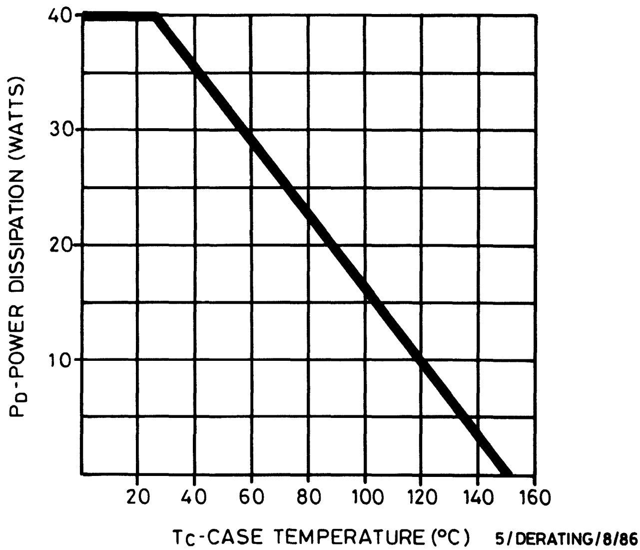


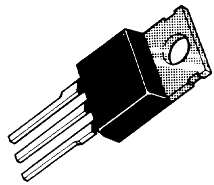
Fig. 13 Power v temperature derating curve

N-channel enhancement mode vertical DMOS FET

IRF630 IRF631 IRF632 IRF633

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-220

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
IRF630	200V	9A	0.4Ω
IRF631	150V	9A	0.4Ω
IRF632	200V	8A	0.6Ω
IRF633	150V	8A	0.6Ω

ABSOLUTE MAXIMUM RATINGS

Parameter		IRF630	IRF631	IRF632	IRF633	Units
V_{DS}	Drain-source voltage	200	150	200	150	V
I_D	Continuous drain current (@ $T_C = 25°C$)	9	9	8	8	A
I_{DM}	Pulse drain current	36	36	32	32	A
V_{GS}	Gate-source voltage	±20	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_C = 25°C$)	75	75	75	75	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150				°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Part No.	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	IRF630 IRF632	200	–	V	$V_{GS} = 0V$, $I_D = 250\mu A$
		IRF631 IRF633	150	–	V	
$V_{GS(th)}$	Gate threshold voltage	All	2	4	V	$V_{GS} = V_{DS}$, $I_D = 250\mu A$
I_{GSS}	Gate-body leakage	All	–	500	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	All	–	250	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		All	–	1000	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	IRF630 IRF631	9	–	A	$V_{DS} = 10V$, $V_{GS} = 10V$
		IRF632 IRF633	8	–	A	
$R_{DS(on)}$	Static drain-source on-state resistance (1)	IRF630 IRF631	–	0.4	Ω	$I_D = 5A$, $V_{GS} = 10V$
		IRF632 IRF633	–	0.6	Ω	
g_{fs}	Forward transconductance (1) (2)	All	3	–	S	$V_{DS} = 10V$, $I_D = 5A$

IRF630 IRF631 IRF632 IRF633

ELECTRICAL CHARACTERISTICS cont.

	Parameter	Part No.	Min.	Max.	Unit	Conditions
C_{iss}	Input capacitance (2)	All	–	800	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	All	–	450	pF	
C_{rss}	Reverse transfer capacitance (2)	All	–	150	pF	
$t_{d(on)}$	Turn-on delay time (2)	All	–	30	ns	$V_{DD} \approx 90V$, $I_D = 5A$ $Z_O = 15\Omega$
t_r	Rise time (2)	All	–	50	ns	
$t_{d(off)}$	Turn-off delay time (2)	All	–	50	ns	
t_f	Fall time (2)	All	–	40	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Part No.	Typ.	Max.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	IRF630 IRF631	–	2.0	V	$V_{GS} = 0V$, $I_S = 9A$ $T_C = 25°C$
		IRF632 IRF633	–	1.8	V	$V_{GS} = 0V$, $I_S = 8A$ $T_C = 25°C$
t_{rr}	Reverse recovery time (2)	All	450	–	ns	$I_F = 9A$, $dI_F/dt = 100A/\mu s$ $T_j = 150°C$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.

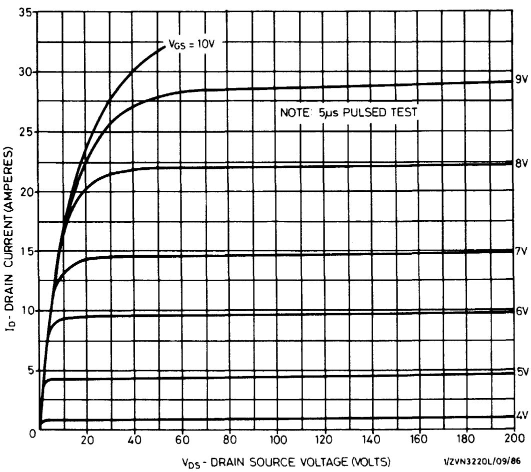


Fig. 1 Typical output characteristics

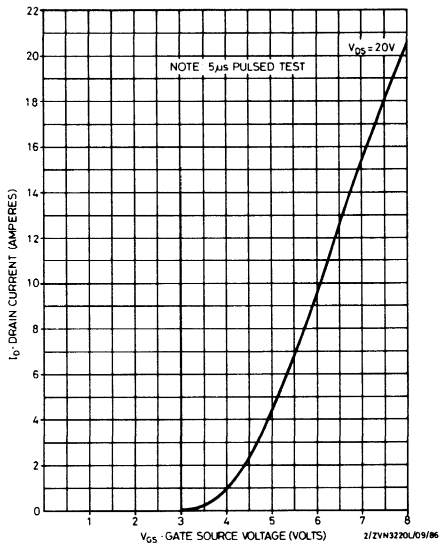


Fig. 2 Typical transfer characteristics

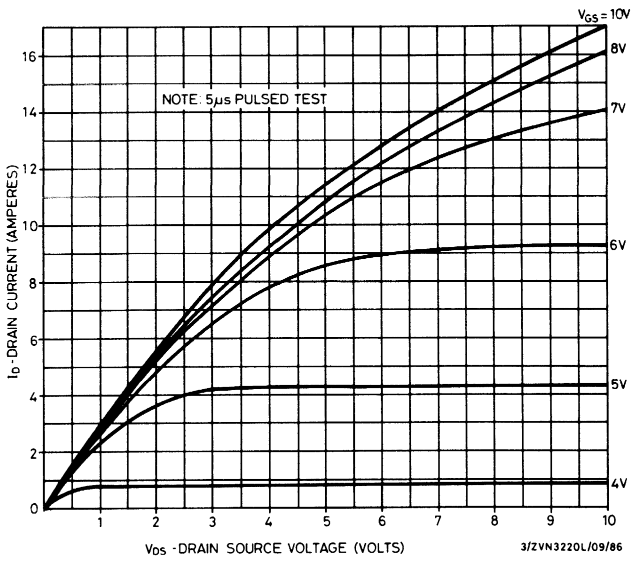


Fig. 3 Typical saturation characteristics

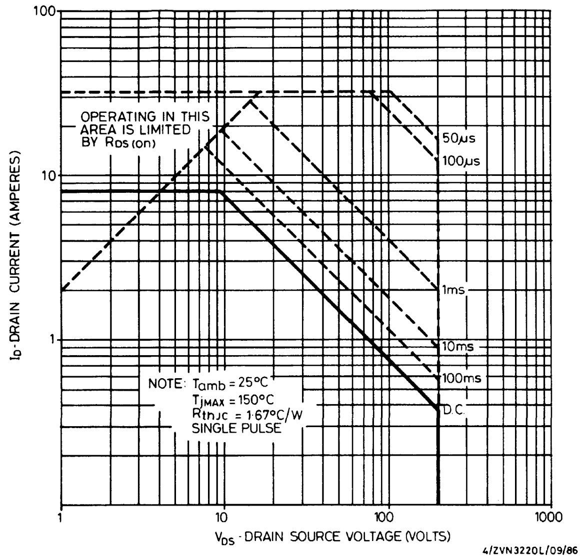


Fig. 4 Maximum safe operating area

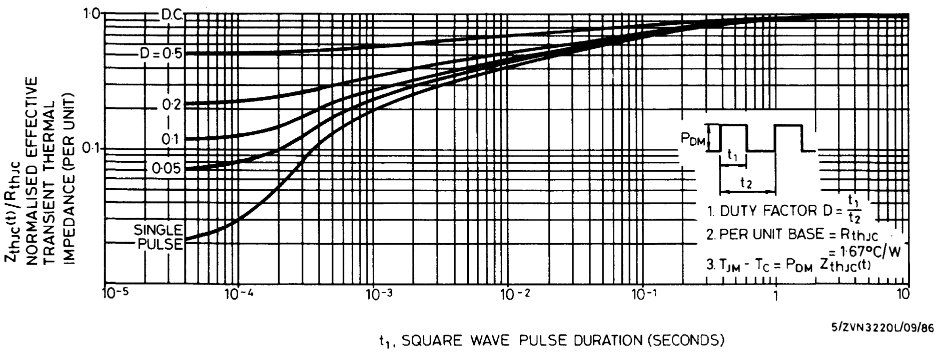


Fig. 5 Maximum effective transient thermal impedance, junction-case v pulse duration

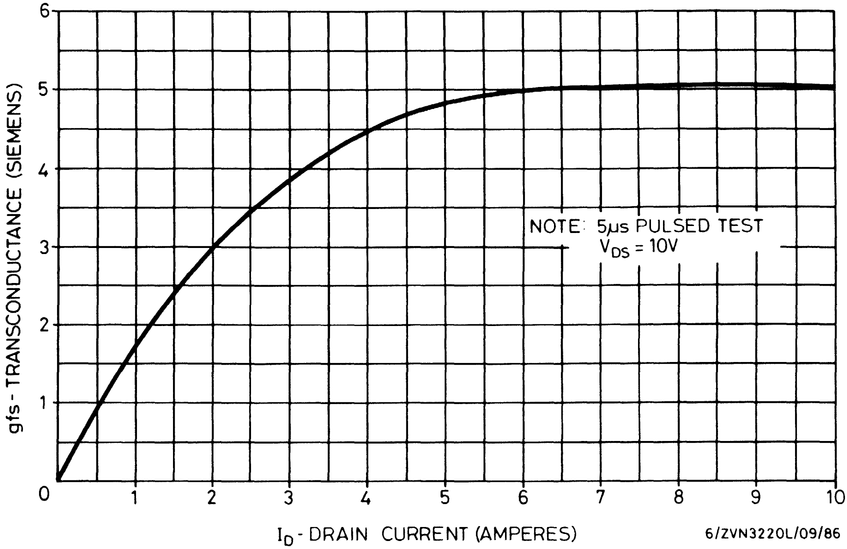


Fig. 6 Typical transconductance v drain current

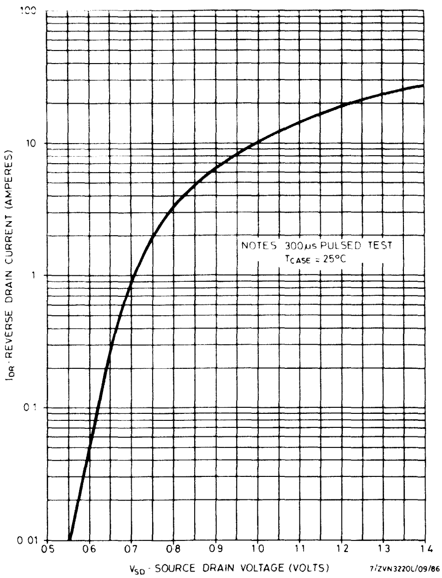


Fig. 7 Typical source-drain diode forward voltage

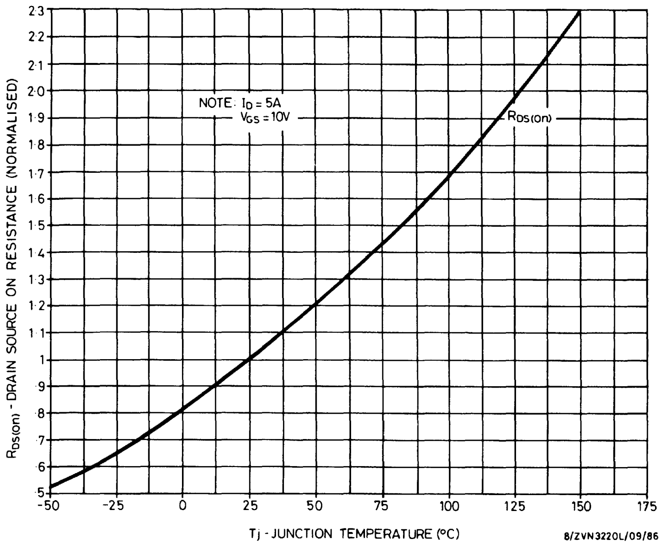


Fig. 8 Normalised on-resistance v temperature

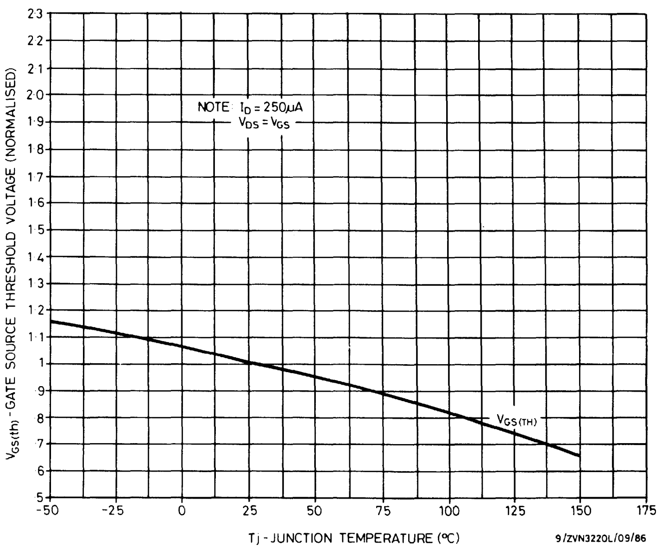


Fig. 9 Normalised gate threshold voltage v temperature

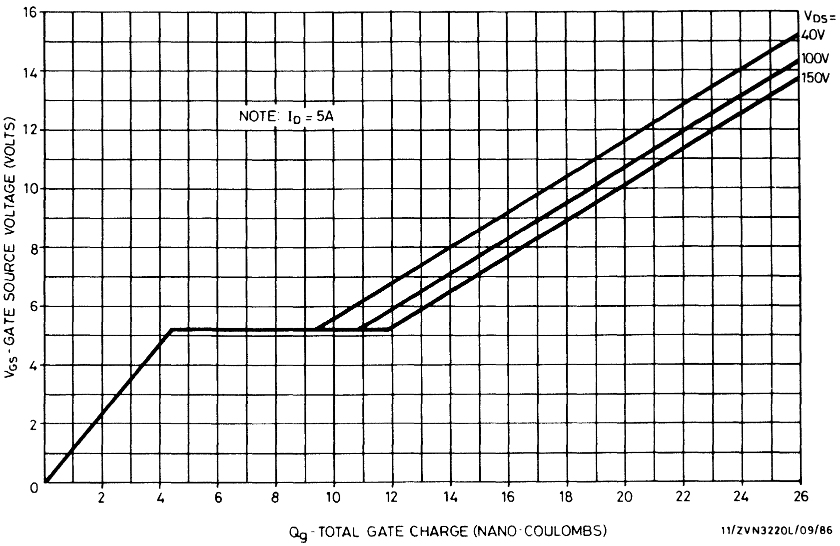


Fig. 10 Typical gate charge v gate-source voltage

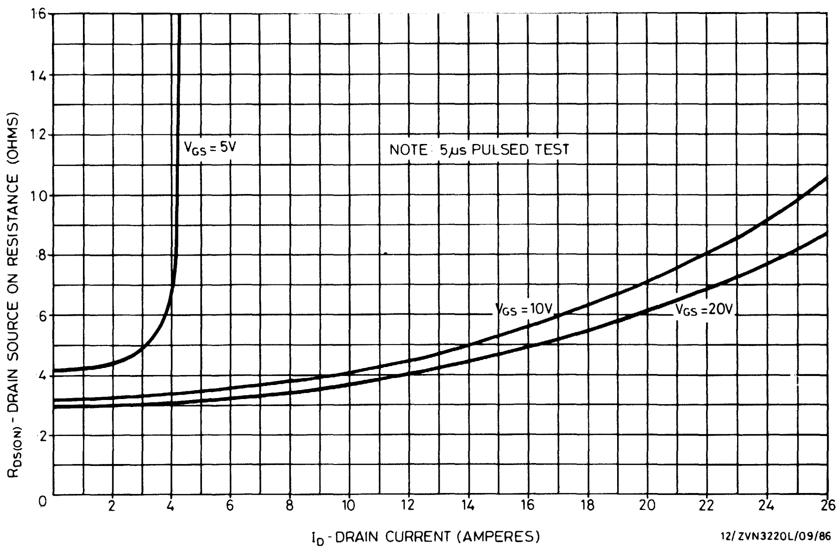


Fig. 11 Typical on-resistance v drain current

IRF630 IRF631 IRF632 IRF633

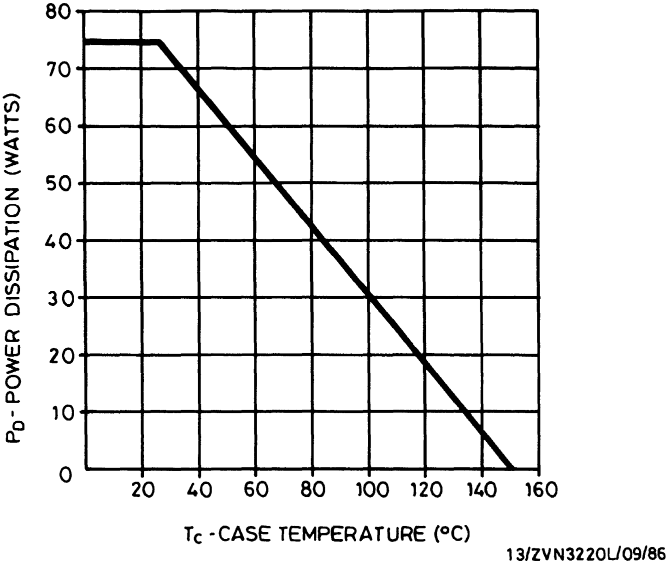


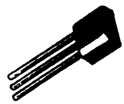
Fig. 12 Power v temperature derating curve

N-channel enhancement mode vertical DMOS FET

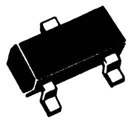
VN10L

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX P



SOT-23
SUFFIX F

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
VN10LP	60V	0.27A	5Ω
VN10LF	60V	0.15A	5Ω

VN10L

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	SOT-23	Units
V_{DS}	Drain-source voltage	60	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.27	0.15	A
I_{DM}	Pulse drain current	3	3	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.25	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	V	$I_D = 100\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	2.5	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
$I_{D(on)}$	On-state drain current (1)	750	–	mA	$V_{DS} = 15V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	5	Ω	$I_D = 500mA$, $V_{GS} = 10V$
		–	7.5	Ω	$I_D = 200mA$, $V_{GS} = 5V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 15V$, $I_D = 500mA$
C_{iss}	Input capacitance (2)	–	60	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{(on)}$	Turn-on time (2) (3)	–	10	ns	$V_{DD} \approx 15V$, $I_D = 0.6A$
$t_{(off)}$	Turn-off time (2) (3)	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator.

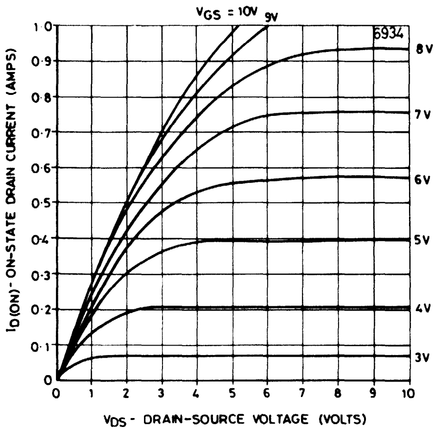


Fig. 1 Typical saturation characteristics

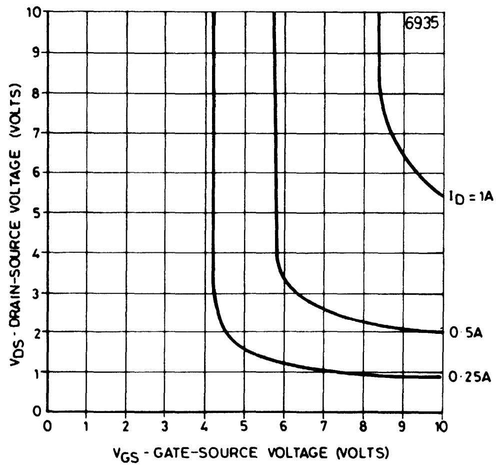


Fig. 2 Typical voltage saturation characteristics

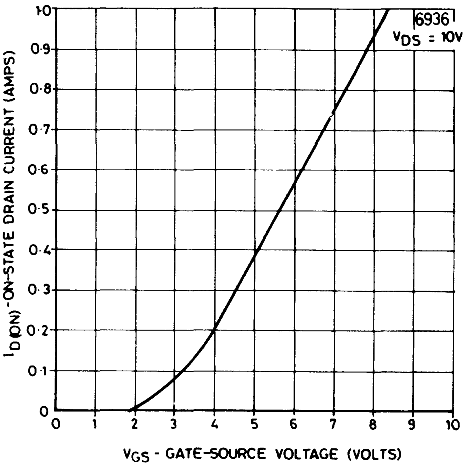


Fig. 3 Typical transfer characteristics

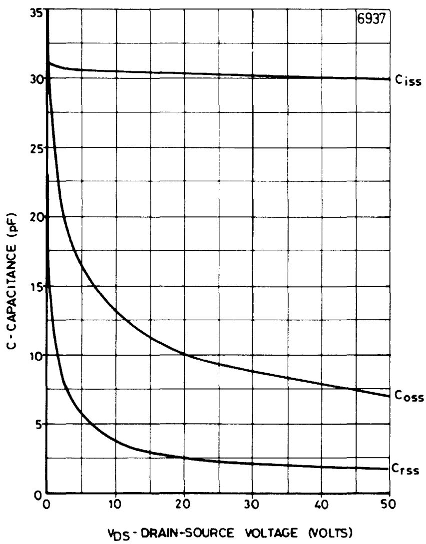


Fig. 4 Typical capacitance v drain-source voltage

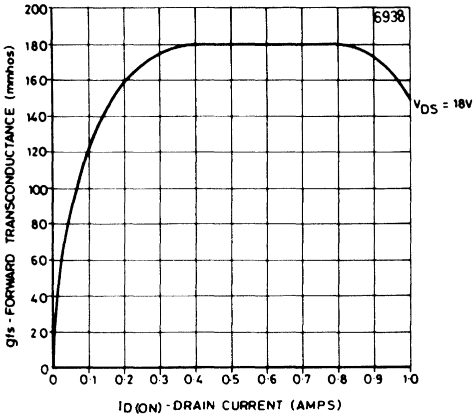


Fig. 5 Typical transconductance v drain current

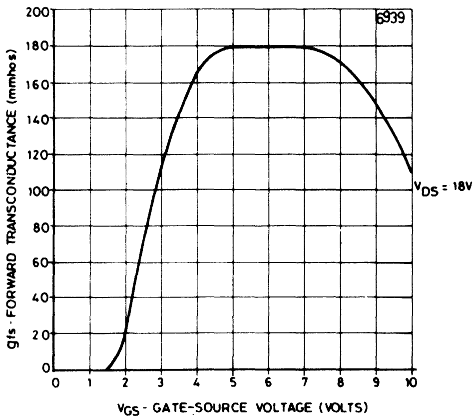


Fig. 6 Typical transconductance v gate-source voltage

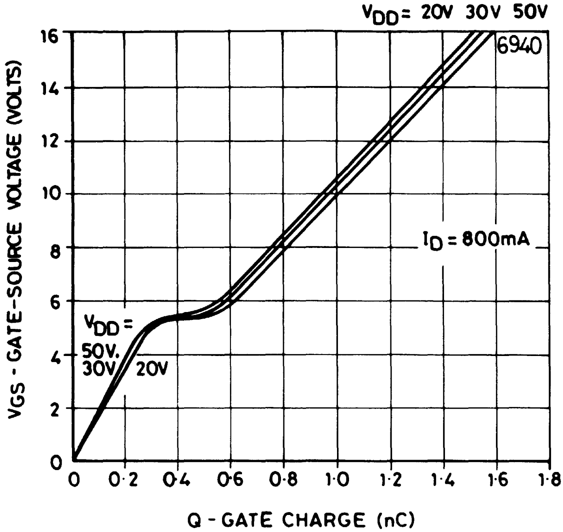


Fig. 7 Typical gate charge v gate-source voltage

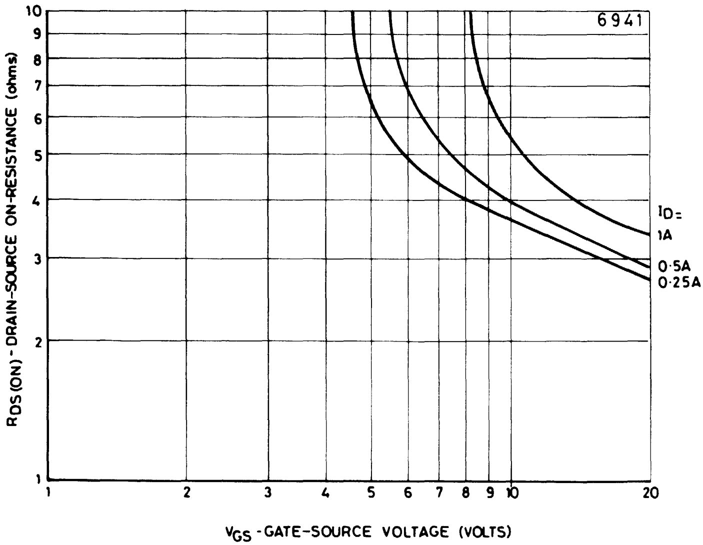


Fig. 8 Typical on-resistance v gate-source voltage

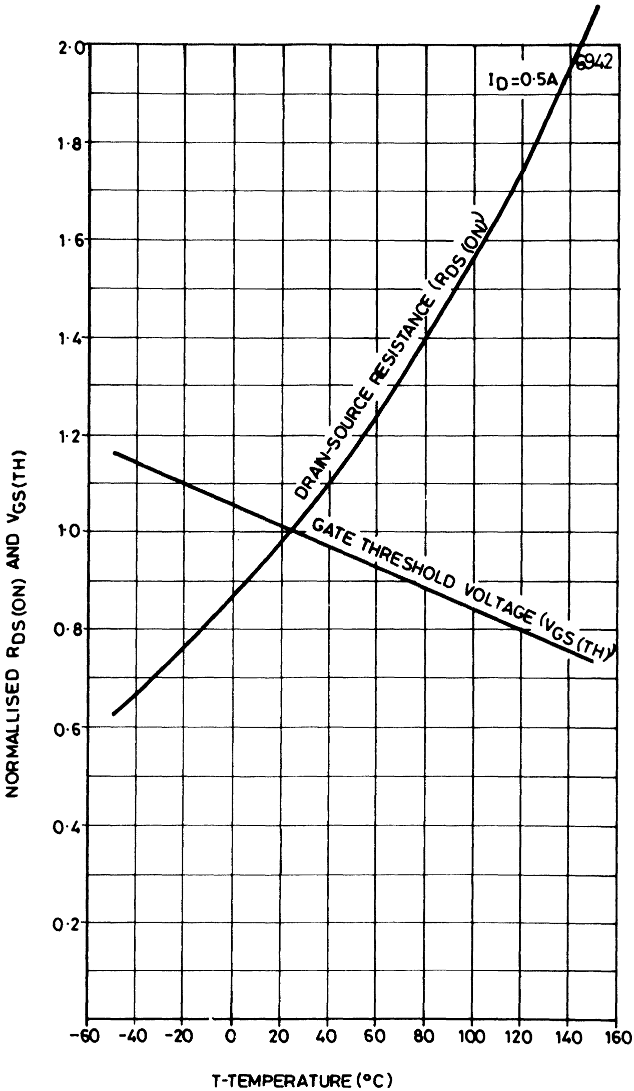


Fig. 9 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

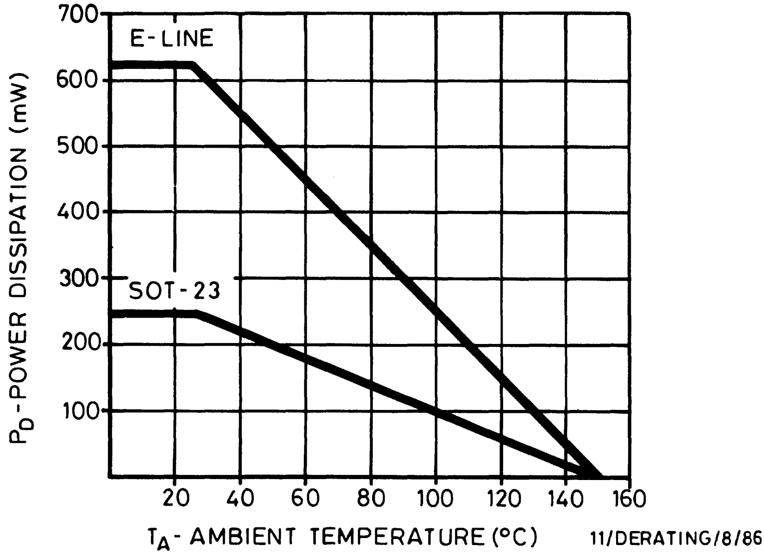


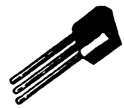
Fig. 10 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

ZVNL120

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVNL120A	200V	0.18A	10Ω

ZVNL120

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.18	A
I_{DM}	Pulse drain current	2	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.5	1.5	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$, (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	500	–	mA	$V_{DS} = 25V$, $V_{GS} = 5V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	10	Ω	$I_D = 250mA$, $V_{GS} = 5V$
		–	10	Ω	$I_D = 125mA$, $V_{GS} = 3V$
g_{fs}	Forward transconductance (1) (2)	200	–	mS	$V_{DS} = 25V$, $I_D = 250mA$
C_{iss}	Input capacitance (2)	–	85	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx 25V$, $I_D = 250mA$
t_r	Rise time (2) (3)	–	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	20	ns	
t_f	Fall time (2) (3)	–	12	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator.

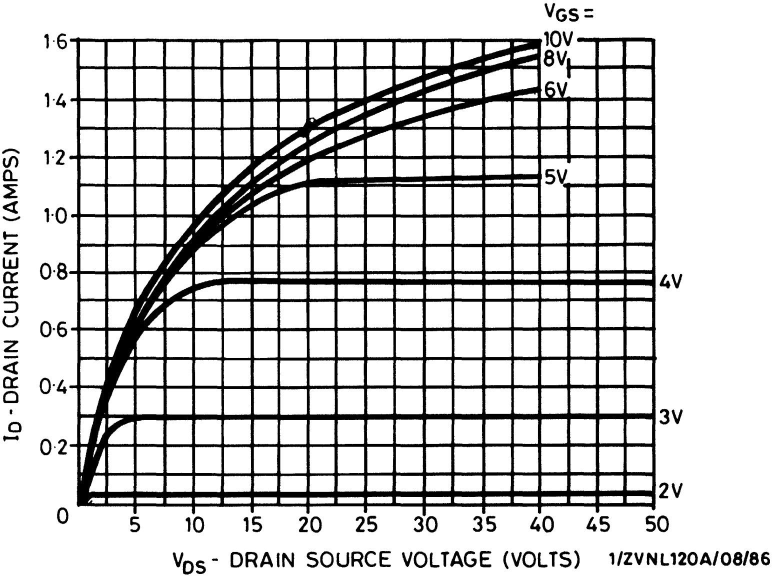


Fig. 1 Typical output characteristics

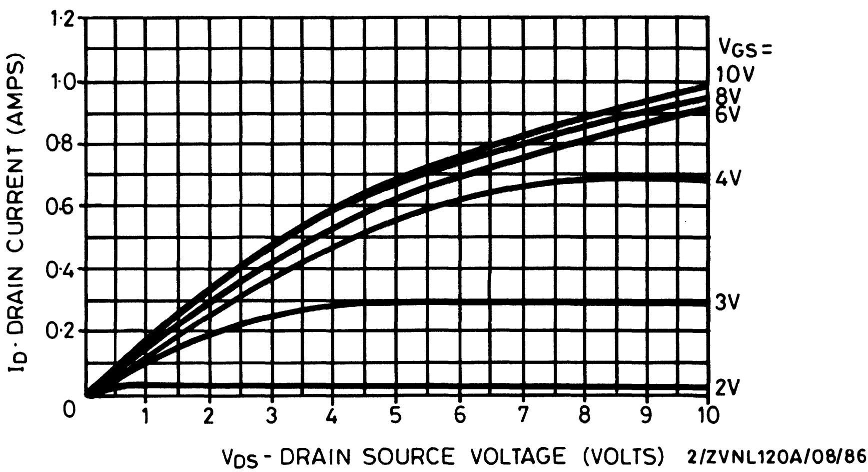


Fig. 2 Typical saturation characteristics

ZVNL120

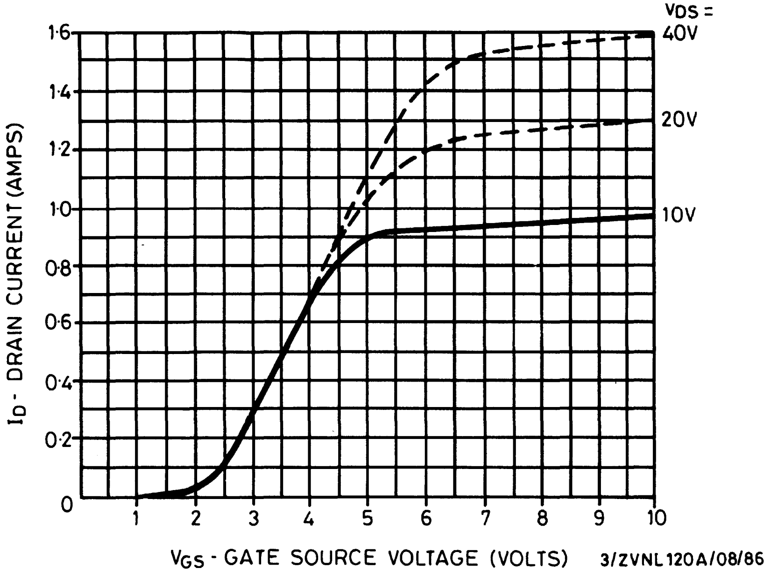


Fig. 3 Typical transfer characteristics

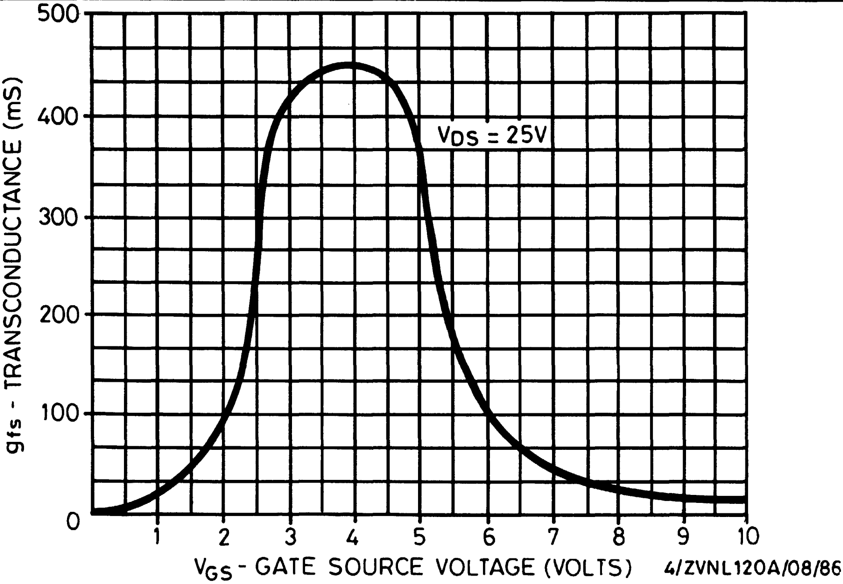


Fig. 4 Typical transconductance v gate-source voltage

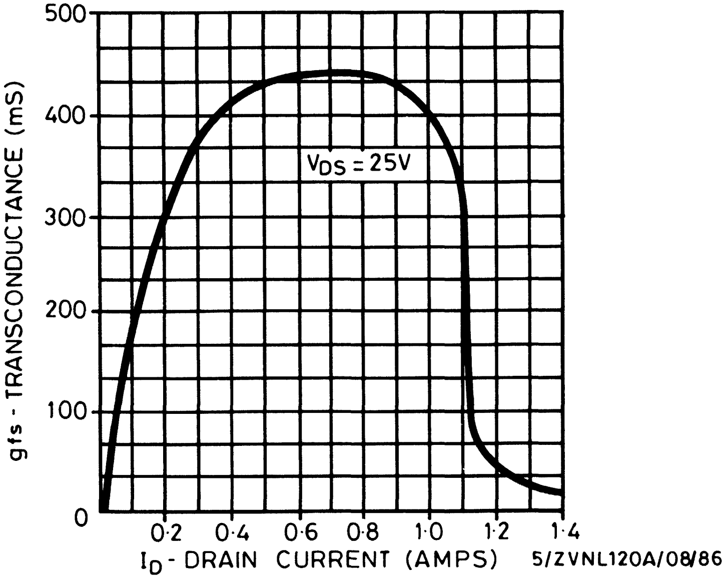


Fig. 5 Typical transconductance v drain current

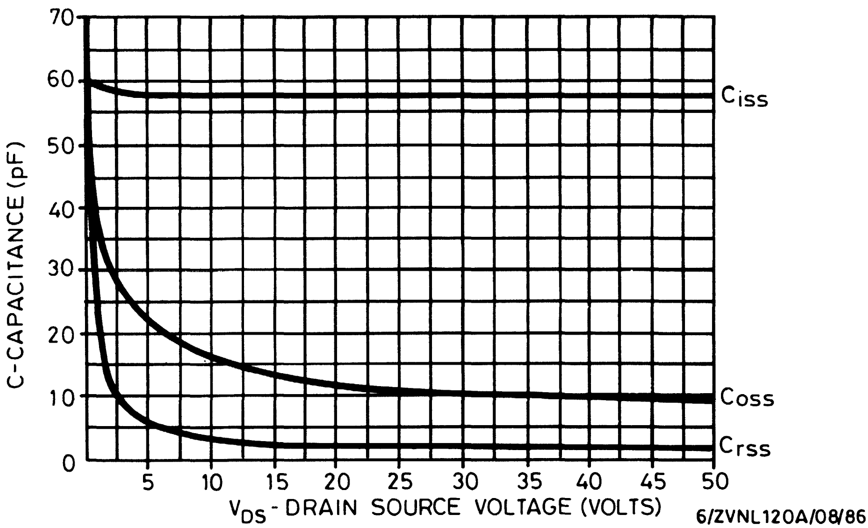


Fig. 6 Typical capacitance v drain-source voltage

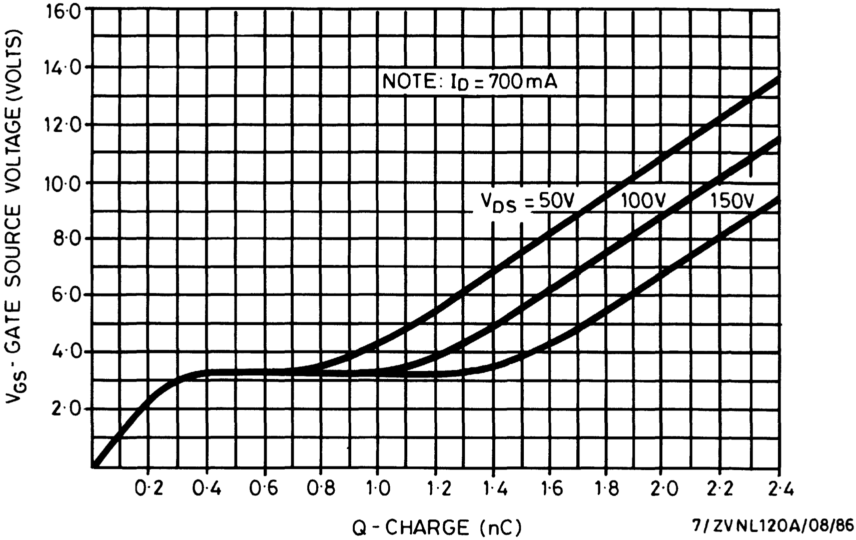


Fig. 7 Typical gate charge v gate-source voltage

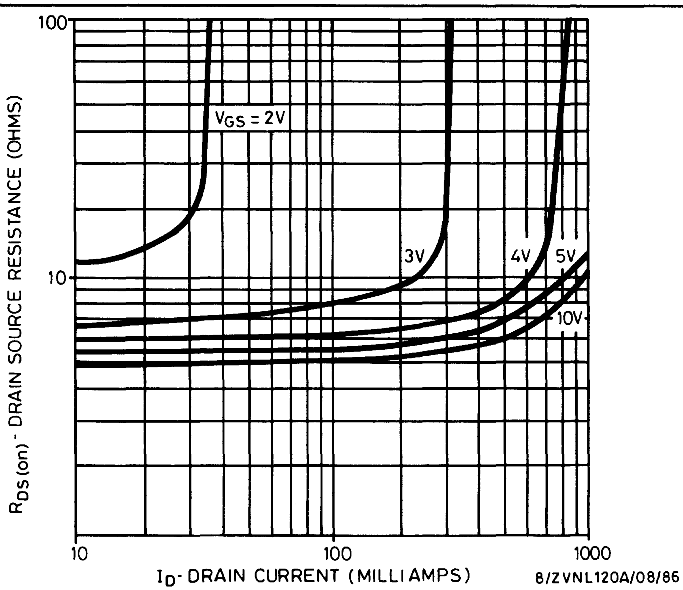


Fig. 8 Typical on-resistance v drain current

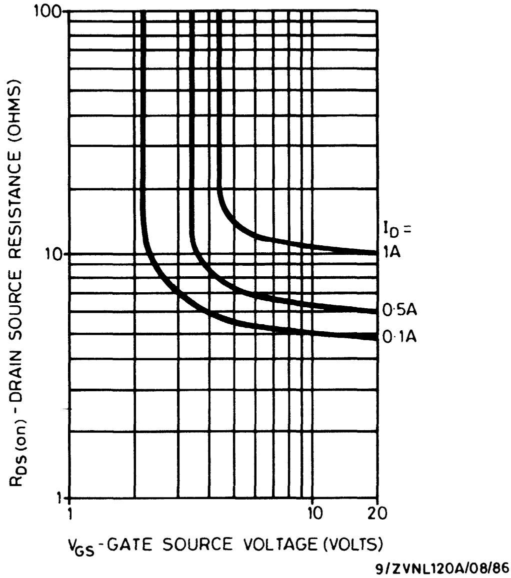


Fig. 9 Typical on-resistance v gate-source voltage

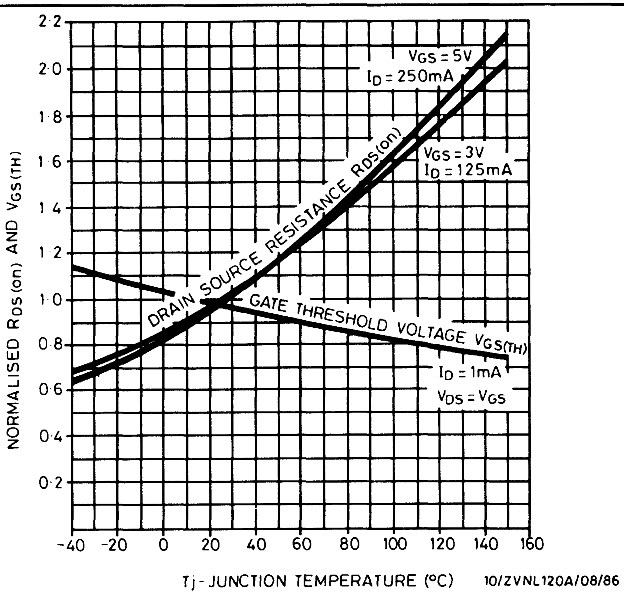


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

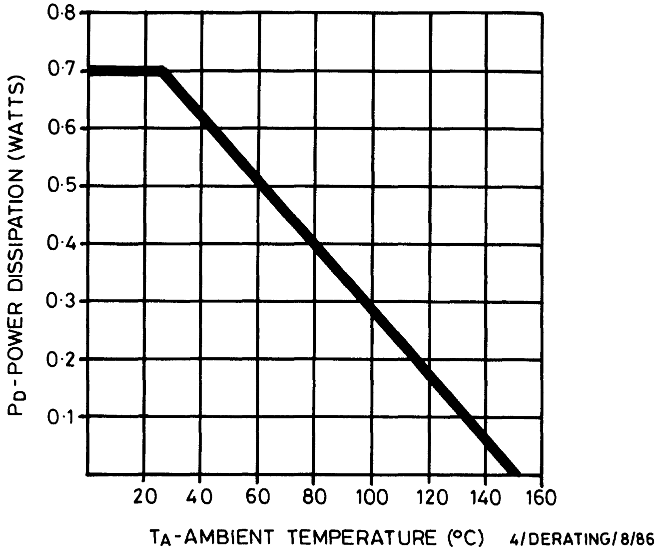


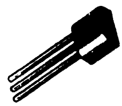
Fig. 11 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

ZVNL535

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVNL535A	350V	0.09A	40Ω

ZVNL535

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09	A
I_{DM}	Pulse drain current	0.8	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	350	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.5	1.5	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	50	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	400	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$, (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	200	–	mA	$V_{DS} = 25V$, $V_{GS} = 5V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	40	Ω	$I_D = 100mA$, $V_{GS} = 5V$
		–	40	Ω	$I_D = 50mA$, $V_{GS} = 3V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	70	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	10	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx 25V$, $I_D = 100mA$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	16	ns	
t_f	Fall time (2) (3)	–	10	ns	

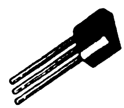
(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement mode vertical DMOS FET

ZVN0117TA

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0117TA	170V	0.16A	23Ω

ZVN0117TA

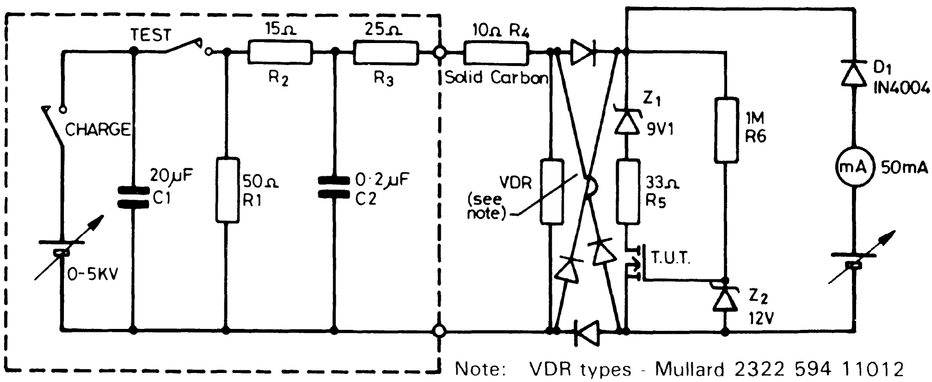
ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	170	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.16	A
I_{DM}	Pulse drain current	2	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	170	–	V	$I_D = 10\mu A$, $V_{GS} = 0V$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS} = \pm 15V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	50	μA	$V_{GS} = 0V$, $V_{DS} = 140V$ $T_A = 50°C$
		(equivalent to 10μA @ 25°C)			
$I_{D(on)}$	On-state drain current (1)	100	–	mA	$V_{DS} = 3V$, $V_{GS} = 3.3V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	23	Ω	$I_D = 100mA$, $V_{GS} = 3.3V$
		–	23	Ω	$I_D = 30mA$, $V_{GS} = 3V$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.



Note: VDR types - Mullard 2322 594 11012
Siemens S10V S07K 75
Matsushita ER2-C070K 10

The transistor under test should withstand a surge applied via above circuit when C1 is charged to 1.5kV.

6872

Fig. 1 Surge test circuit

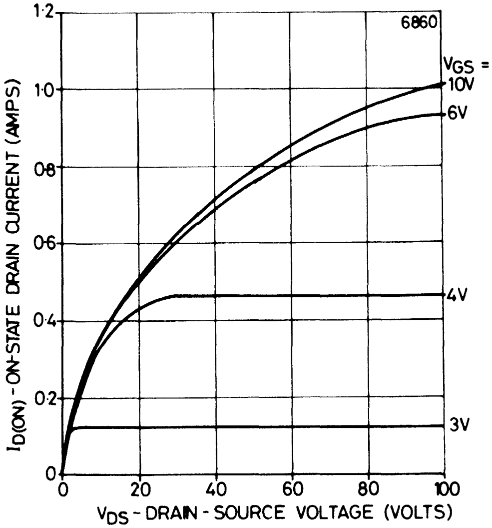


Fig. 2 Typical output characteristics

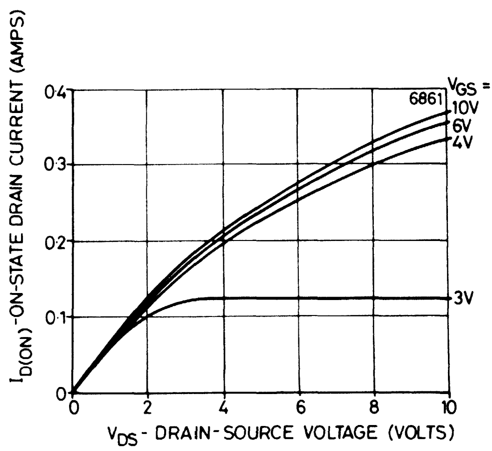


Fig. 3 Typical saturation characteristics

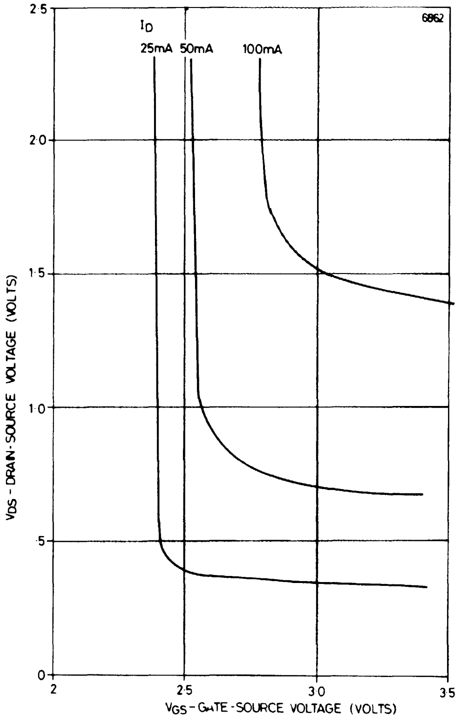


Fig. 4 Typical voltage saturation characteristics

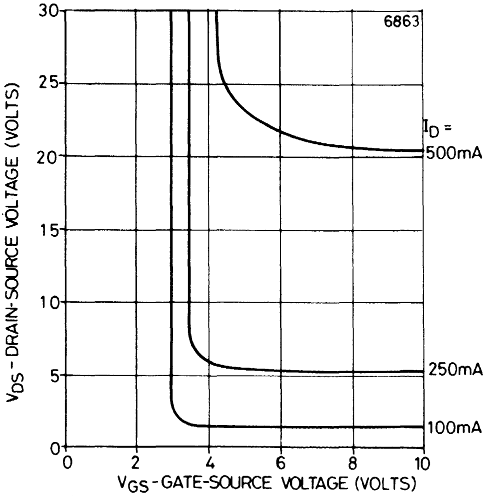


Fig. 5 Typical voltage saturation characteristics

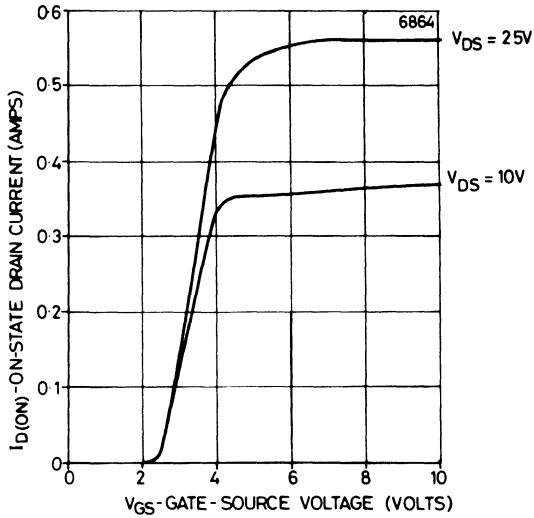


Fig. 6 Typical transfer characteristics

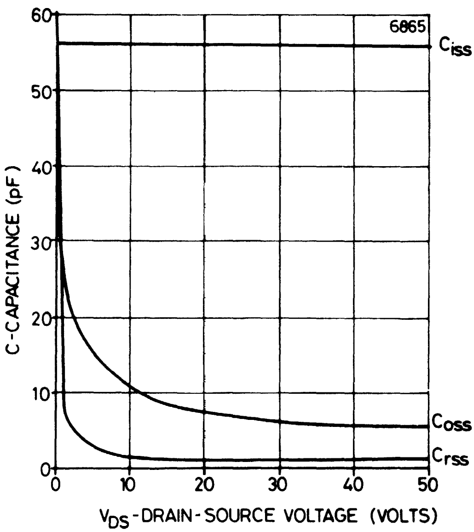


Fig. 7 Typical capacitance v drain-source voltage

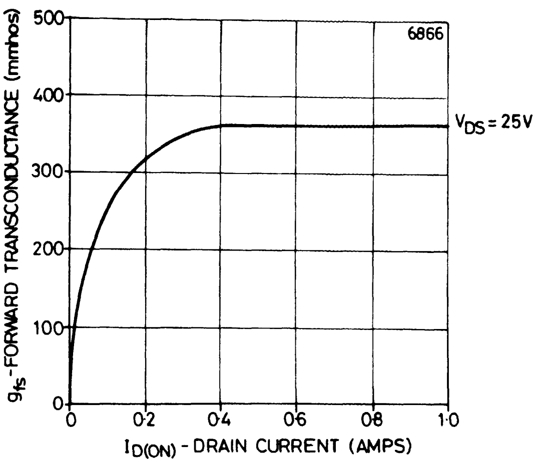


Fig. 8 Typical transconductance v drain current

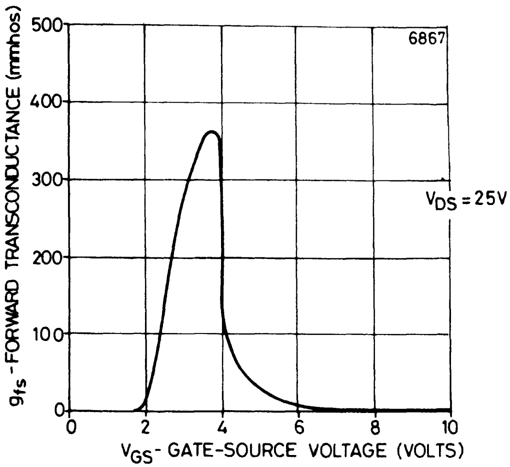


Fig. 9 Typical transconductance v gate-source voltage

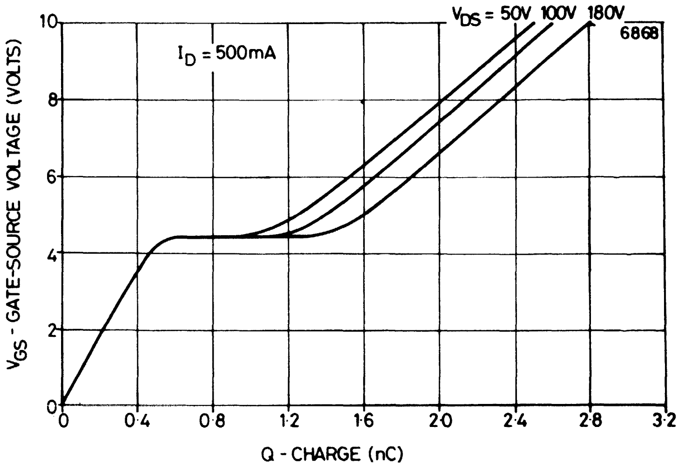


Fig. 10 Typical gate charge v gate-source voltage

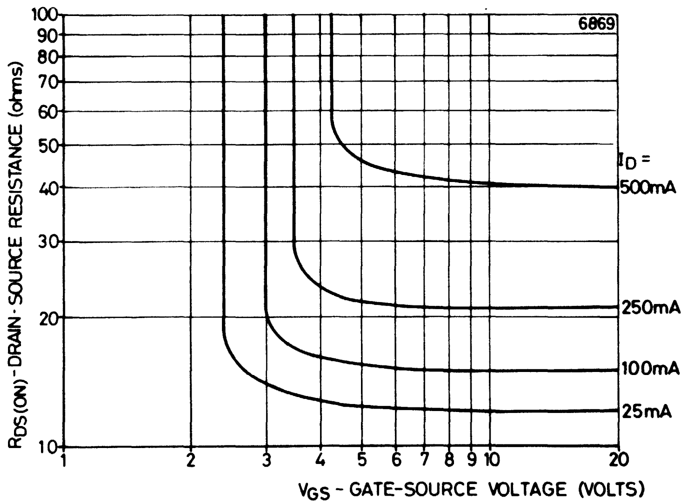


Fig. 11 Typical on-resistance v gate-source voltage

ZVN0117TA

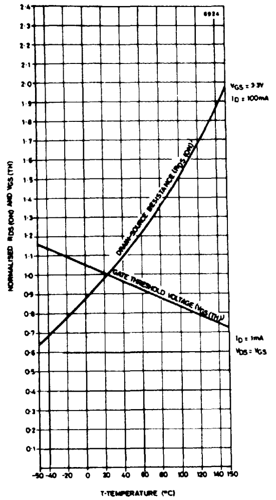


Fig. 12 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

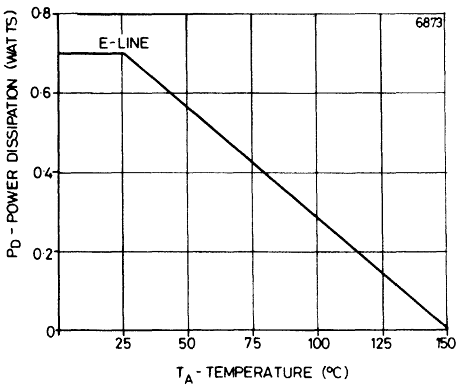


Fig. 13 Power v temperature derating curve (ambient)

N-channel enhancement-mode vertical DMOS FET

ZVN0120

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

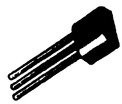
DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

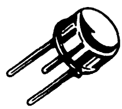
PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0120A	200V	0.16A	16Ω
ZVN0120B	200V	0.42A	16Ω
ZVN0120L*	200V	0.5A	16Ω

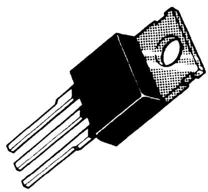
*BS-CECC approved.



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVN0120

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	200	200	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.16	0.16	0.23	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.42	0.5	A
I_{DM}	Pulse drain current	2	2	2	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	–	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	0.5	1	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	16	Ω	$I_D = 0.25A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	0.1	0.25	–	S	$V_{DS} = 25V$, $I_D = 0.25A$
C_{iss}	Input capacitance (2)	–	62	85	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	9	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	2	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3	7	ns	$V_{DD} \approx 25V$, $I_D = 0.25A$
t_r	Rise time (2) (3)	–	2	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	11	16	ns	
t_f	Fall time (2) (3)	–	5	8	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Forward ON voltage (1)	0.76	V	$V_{GS}=0V$, $I_S=0.16A$
t_{rr}	Reverse recovery time	105	ns	$V_{GS}=0V$, $I_F=0.16A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

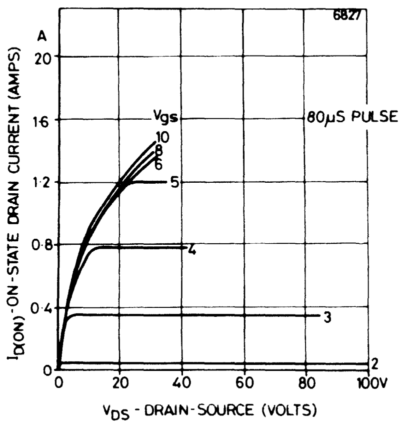


Fig. 1 Typical output characteristics

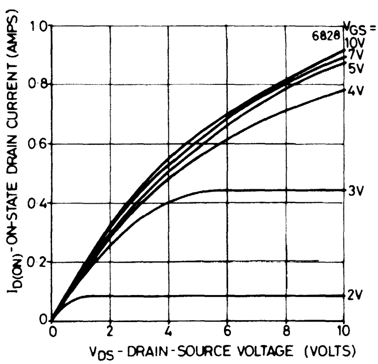


Fig. 2 Typical saturation characteristics

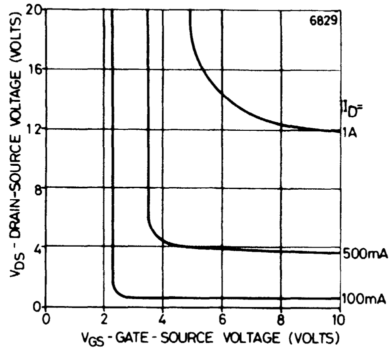


Fig. 3 Typical voltage saturation characteristics

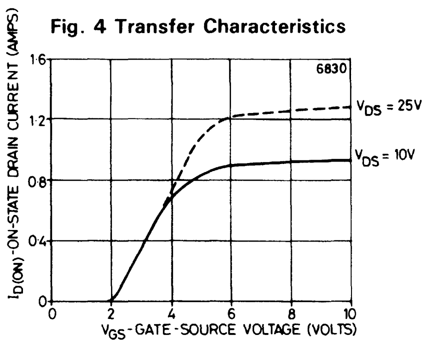


Fig. 4 Typical transfer characteristics

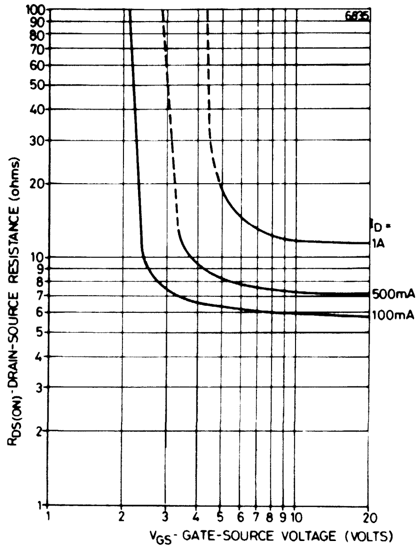


Fig. 5 Typical on-resistance v gate-source voltage

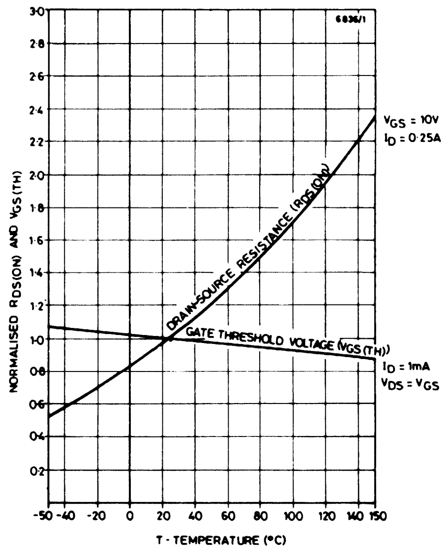


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

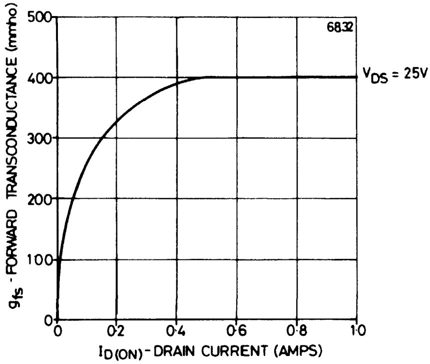


Fig. 7 Typical transconductance v drain current

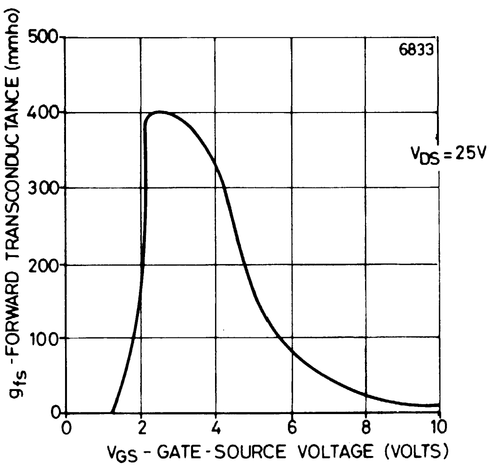


Fig. 8 Typical transconductance v gate-source voltage

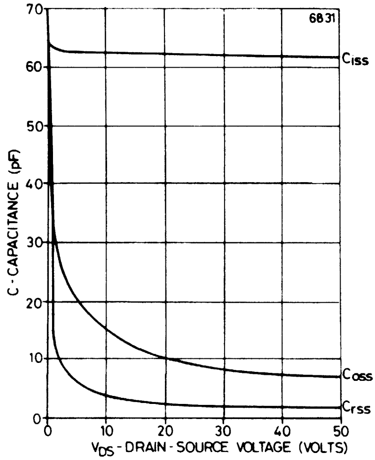


Fig. 9 Typical capacitance v drain-source voltage

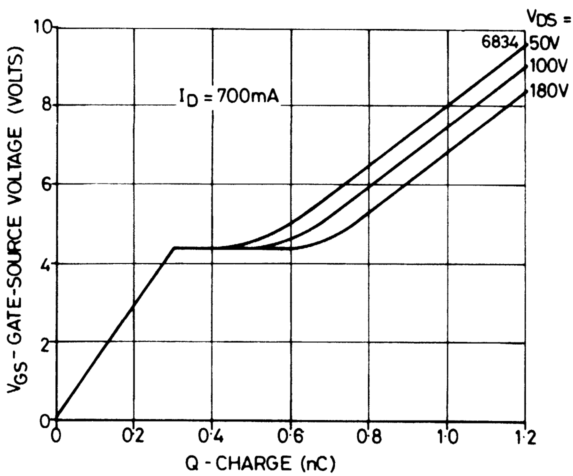


Fig. 10 Typical gate charge v gate-source voltage

ZVN0120

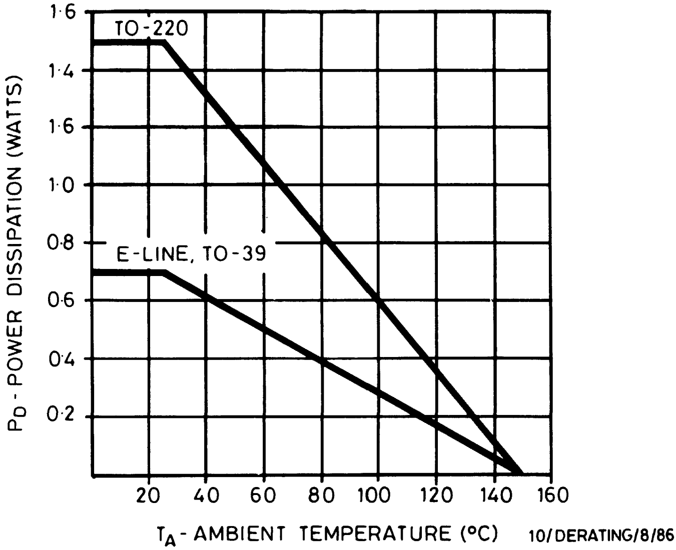


Fig. 11 Power v temperature derating curve (ambient)

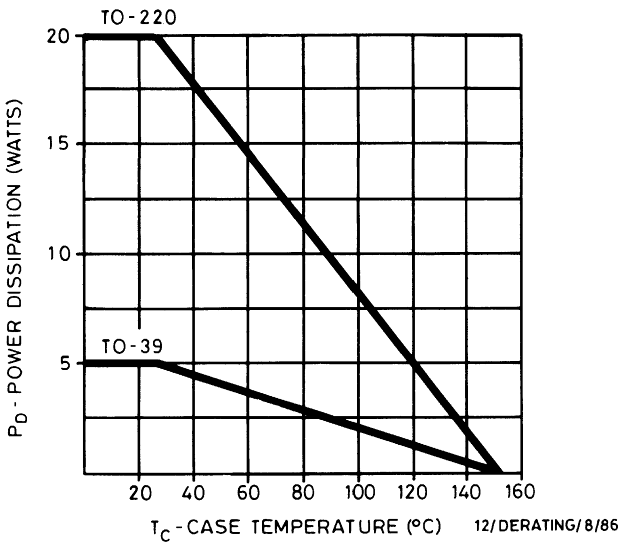


Fig. 12 Power v temperature derating curve (case)

N-channel enhancement-mode vertical DMOS FET

ZVN0124

FEATURES

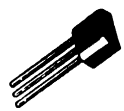
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

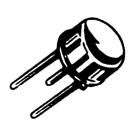
A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

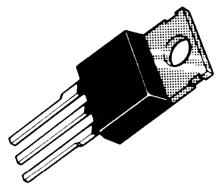
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0124A	240V	0.16A	16Ω
ZVN0124B	240V	0.42A	16Ω
ZVN0124L	240V	0.5A	16Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVN0124

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	240	240	240	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.16	0.16	0.23	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.42	0.5	A
I_{DM}	Pulse drain current	2	2	2	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	240	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	–	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	0.5	1	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	16	Ω	$I_D = 0.25A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	0.1	0.25	–	S	$V_{DS} = 25V$, $I_D = 0.25A$
C_{iss}	Input capacitance (2)	–	62	85	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	9	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	2	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3	7	ns	$V_{DD} \approx 25V$, $I_D = 0.25A$
t_r	Rise time (2) (3)	–	2	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	11	16	ns	
t_f	Fall time (2) (3)	–	5	8	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Forward ON voltage (1)	0.76	V	$V_{GS}=0V$, $I_S=0.16A$
t_{rr}	Reverse recovery time	105	ns	$V_{GS}=0V$, $I_F=0.16A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

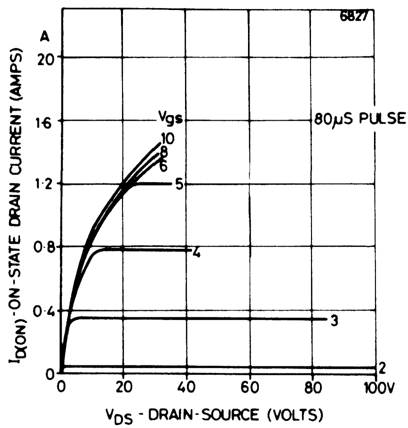


Fig. 1 Typical output characteristics

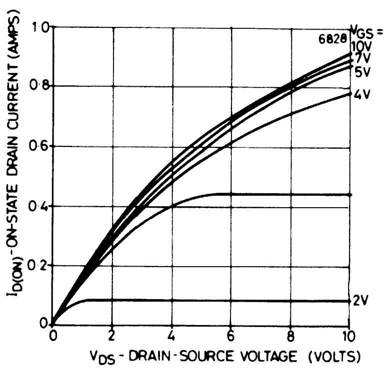


Fig. 2 Typical saturation characteristics

ZVN0124

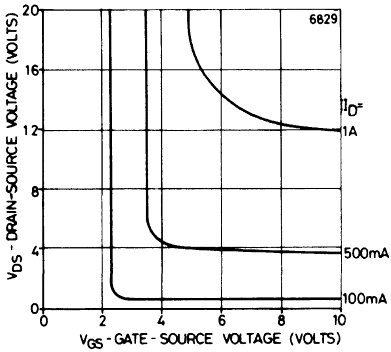


Fig. 3 Typical voltage saturation characteristics

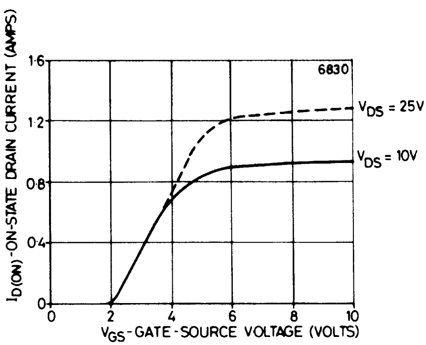


Fig. 4 Typical transfer characteristics

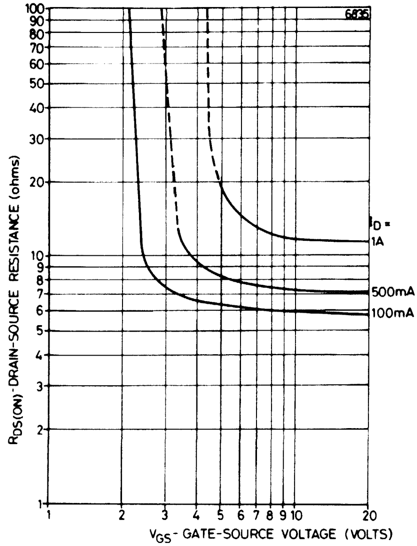


Fig. 5 Typical on-resistance v gate-source voltage

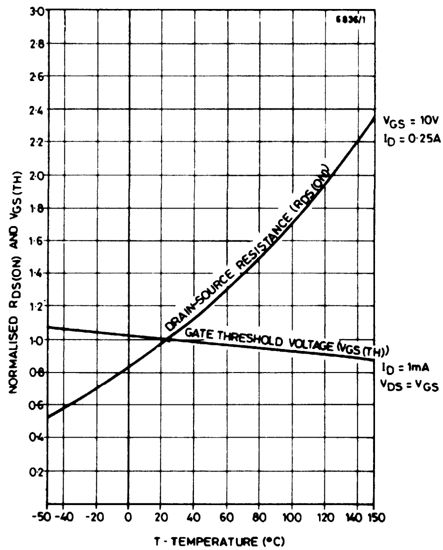


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

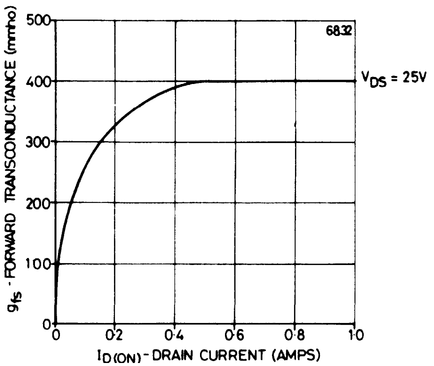


Fig. 7 Typical transconductance v drain current

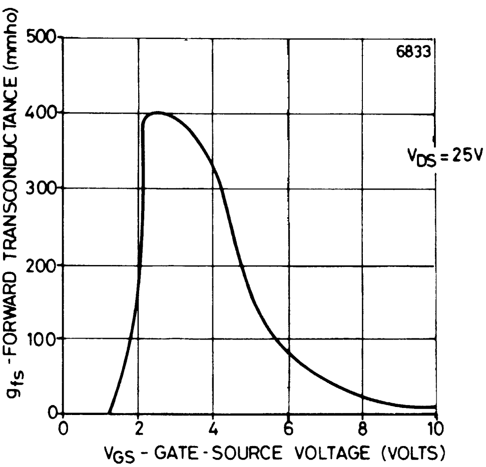


Fig. 8 Typical transconductance v gate-source voltage

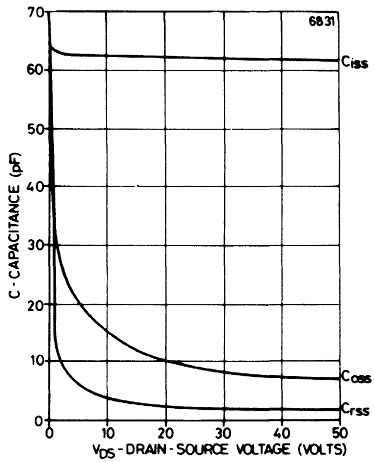


Fig. 9 Typical capacitance v drain-source voltage

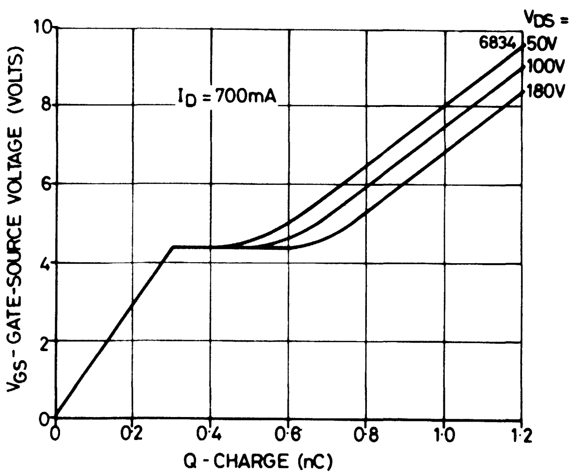


Fig. 10 Typical gate charge v gate-source voltage

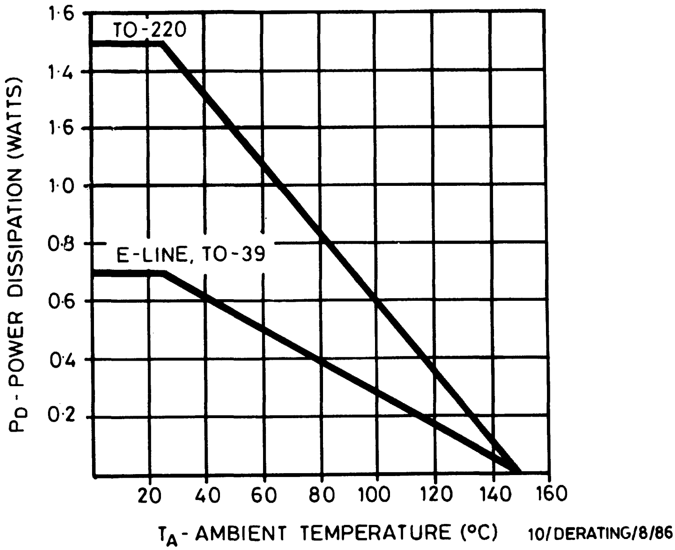


Fig. 11 Power v temperature derating curve (ambient)

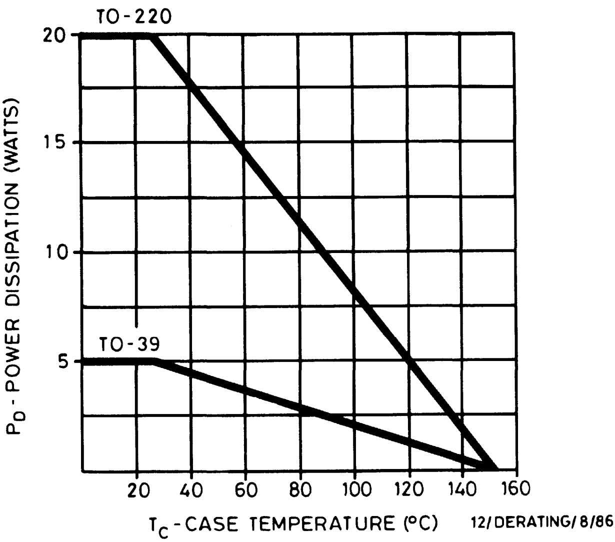


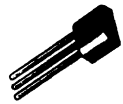
Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

ZVN0535

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0535A*	350V	90mA	50Ω

*BS-CECC approved

ZVN0535

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	Unit
V_{DS}	Drain-source voltage	350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09	A
I_{DM}	Pulse drain current	0.6	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	350	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	400	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	150	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	50	Ω	$I_D = 100mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	70	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	10	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx 25V$, $I_D = 100mA$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	16	ns	
t_f	Fall time (2) (3)	–	10	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.74	V	$V_{GS}=0V$, $I_S=90mA$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

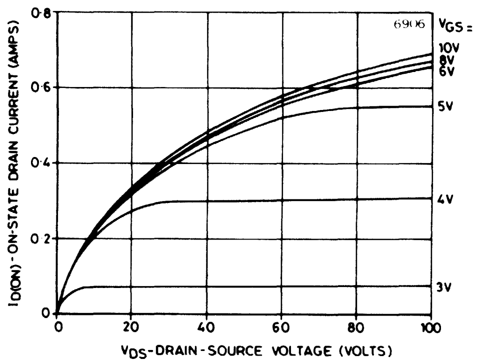


Fig. 1 Typical output characteristics

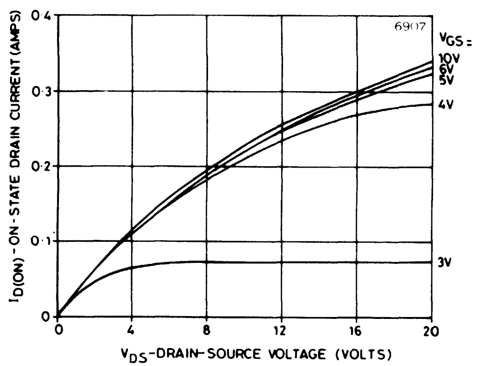


Fig. 2 Typical saturation characteristics

ZVN0535

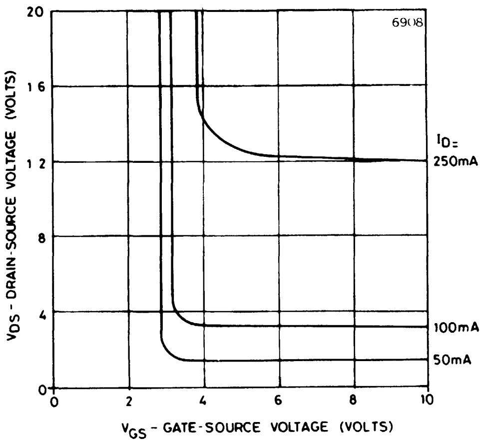


Fig. 3 Typical voltage saturation characteristics

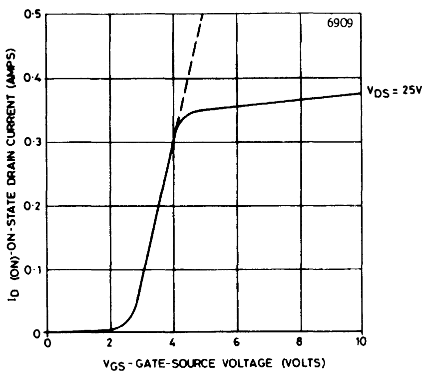


Fig. 4 Typical transfer characteristics

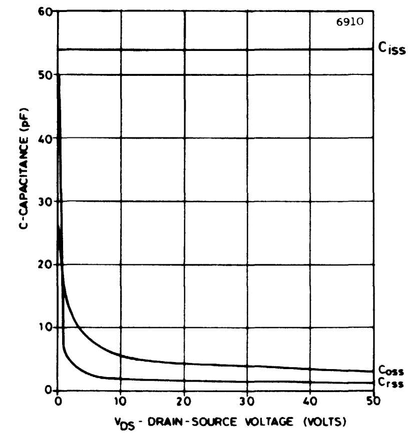


Fig. 5 Typical capacitance v drain-source voltage

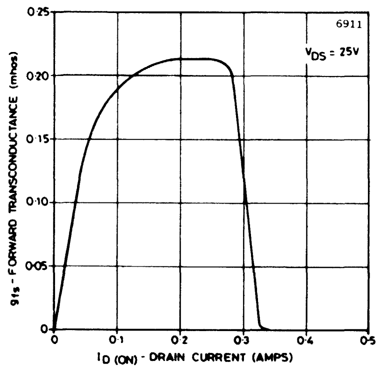


Fig. 6 Typical transconductance v drain current

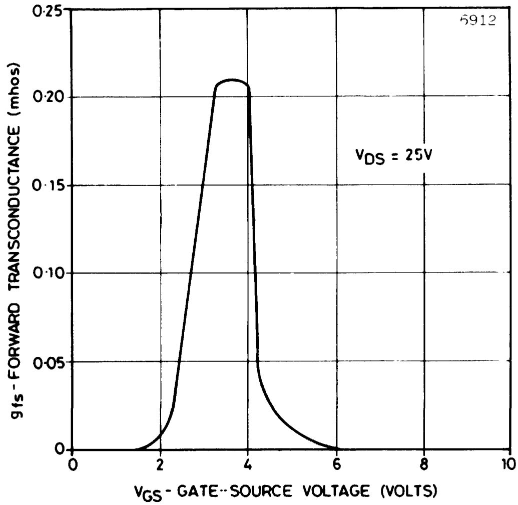


Fig. 7 Typical transconductance v gate-source voltage

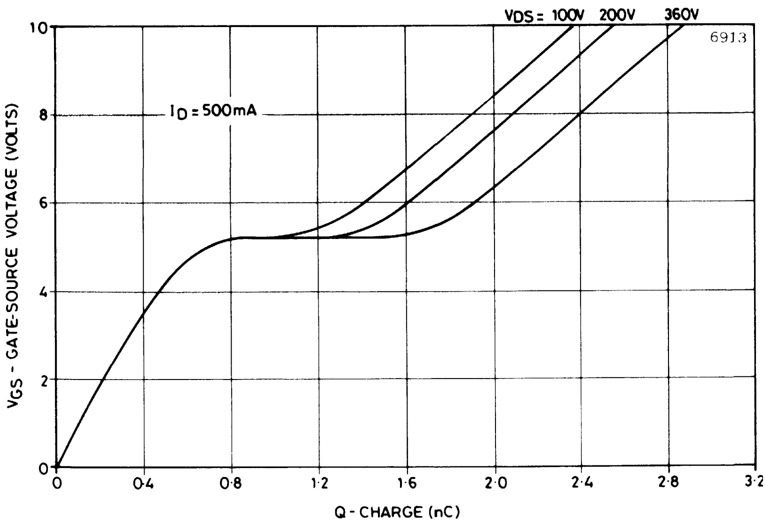


Fig. 8 Typical gate charge v gate-source voltage

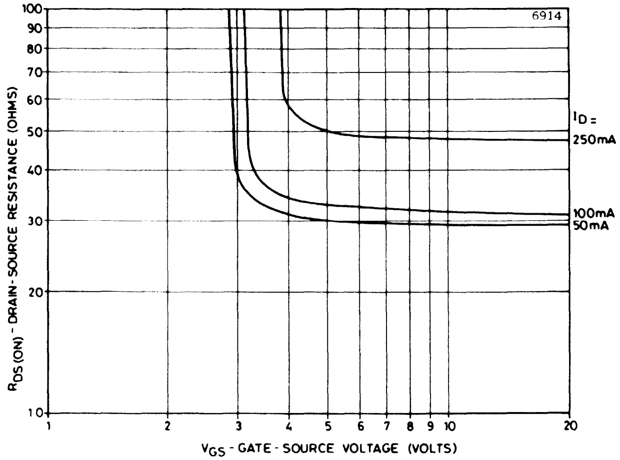


Fig. 9 Typical on-resistance v gate-source voltage

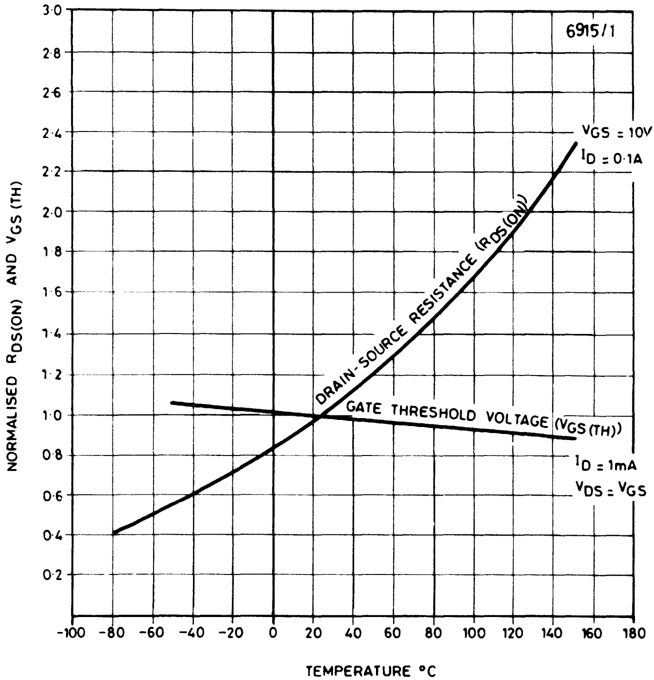


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

ZVN0535

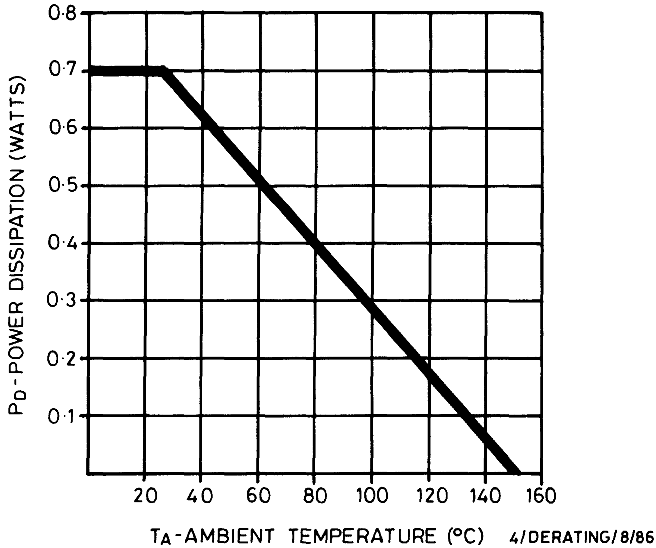


Fig. 11 Power v temperature derating curve (ambient)

N-channel enhancement-mode vertical DMOS FET

ZVN0540

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

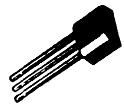
DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

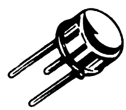
PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0540A*	400V	0.09A	50Ω
ZVN0540B	400V	0.15A	50Ω
ZVN0540L	400V	0.15A	50Ω

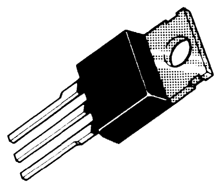
*BS-CECC approved.



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVN0540

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	400	400	400	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09	0.09	0.13	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.15	0.15	A
I_{DM}	Pulse drain current	0.6	0.6	0.6	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	400	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	400	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	150	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	50	Ω	$I_D = 100mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	70	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	10	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx 25V$, $I_D = 0.1A$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	16	ns	
t_f	Fall time (2) (3)	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement-mode vertical DMOS FET

ZVN0545

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

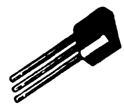
DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

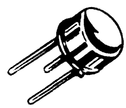
PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN0545A*	450V	0.09A	50Ω
ZVN0545B	450V	0.15A	50Ω
ZVN0545L	450V	0.15A	50Ω

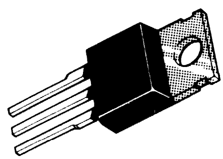
*BS-CECC approved.



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVN0545

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	450	450	450	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09	0.09	0.13	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.15	0.15	A
I_{DM}	Pulse drain current	0.6	0.6	0.6	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	450	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	400	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	150	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	50	Ω	$I_D = 100mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	70	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	10	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx 25V$, $I_D = 0.1A$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	16	ns	
t_f	Fall time (2) (3)	–	10	ns	

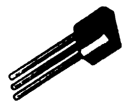
(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement mode vertical DMOS FET

ZVN1409

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN1409A	90V	10mA	250Ω

ZVN1409

ABSOLUTE MAXIMUM RATINGS

Parameter		E-line	Unit
V_{DS}	Drain-source voltage	90	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.01	A
I_{DM}	Pulse drain current	0.04	A
V_{GS}	Gate-source voltage	± 20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	W
T_j, T_{stg}	Operating/storage temperature range	-55 to $+150$	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	90	–	–	V	$I_D = 0.1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D = 0.1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	1	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	10	–	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	250	Ω	$I_D = 5mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	2	–	–	mS	$V_{DS} = 25V$, $I_D = 10mA$
C_{iss}	Input capacitance (2)	–	–	6.5	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	–	3	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	0.65	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	0.3	–	ns	$V_{DD} \approx 25V$, $I_D = 5mA$
t_r	Rise time (2) (3)	–	0.5	–	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	0.35	–	ns	
t_f	Fall time (2) (3)	–	0.5	–	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance on a pulse generator.

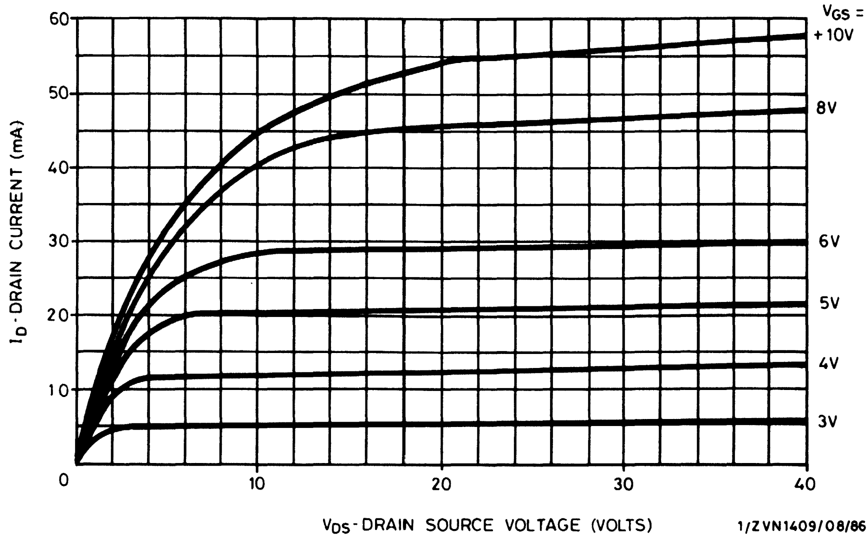


Fig. 1 Typical output characteristics

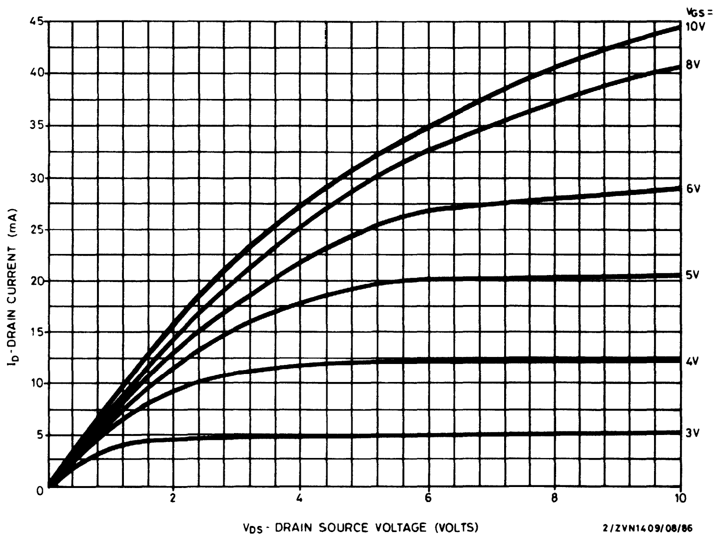


Fig. 2 Typical saturation characteristics

ZVN1409

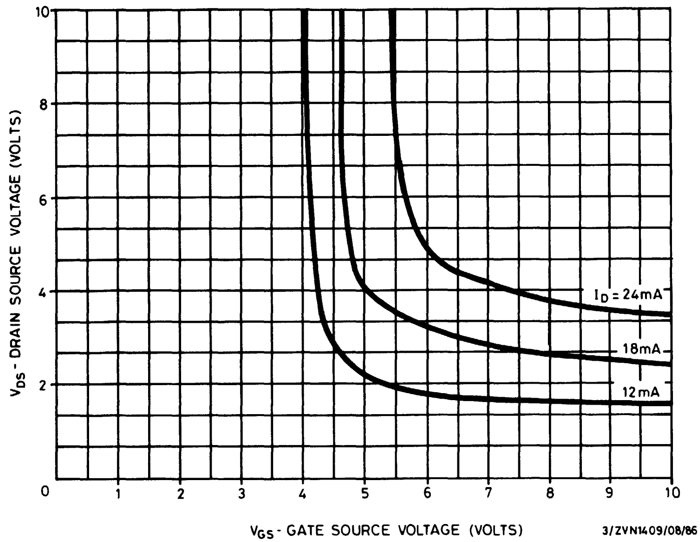


Fig. 3 Typical voltage saturation characteristics

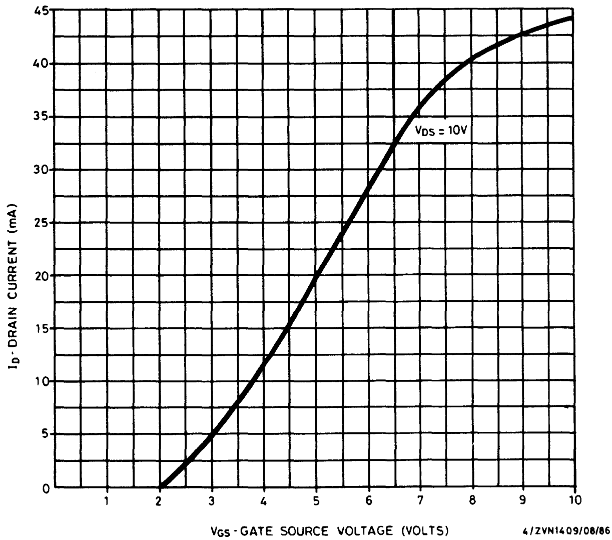


Fig. 4 Typical transfer characteristics

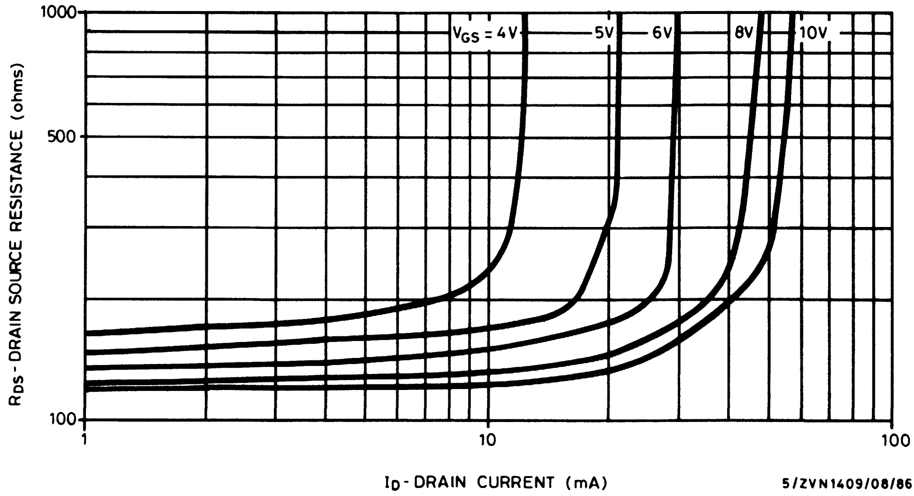


Fig. 5 Typical on-resistance v drain current

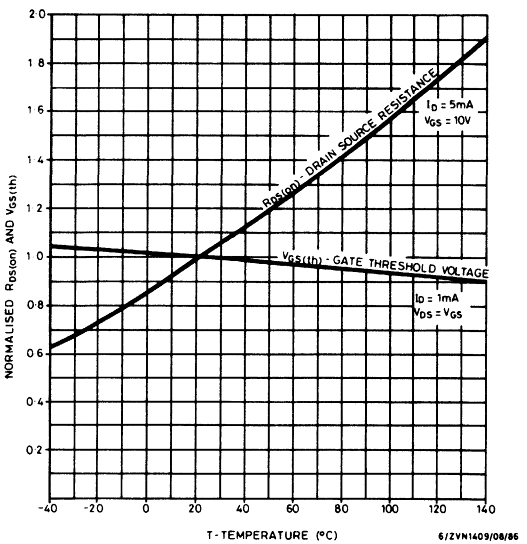


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

ZVN1409

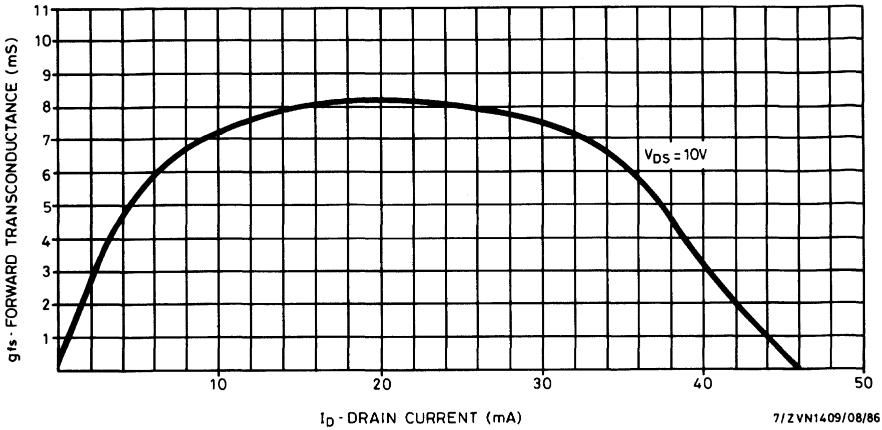


Fig. 7 Typical transconductance v drain current

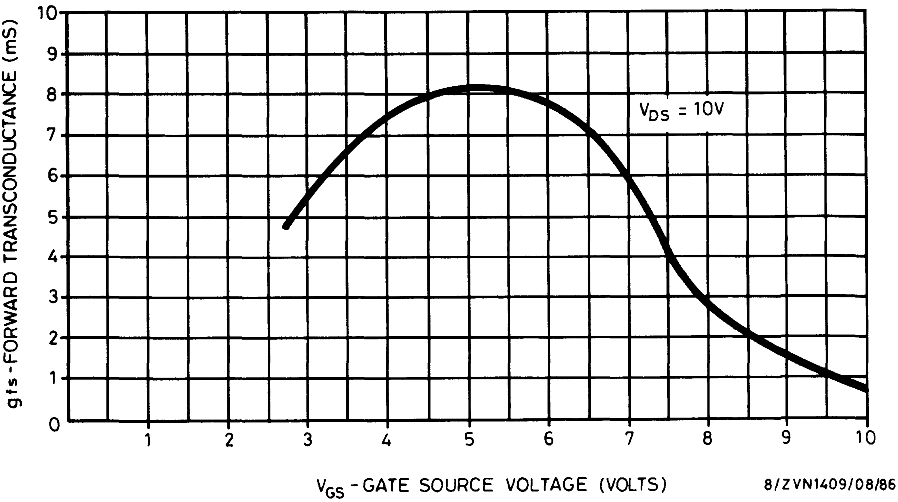


Fig. 8 Typical transconductance v gate-source voltage

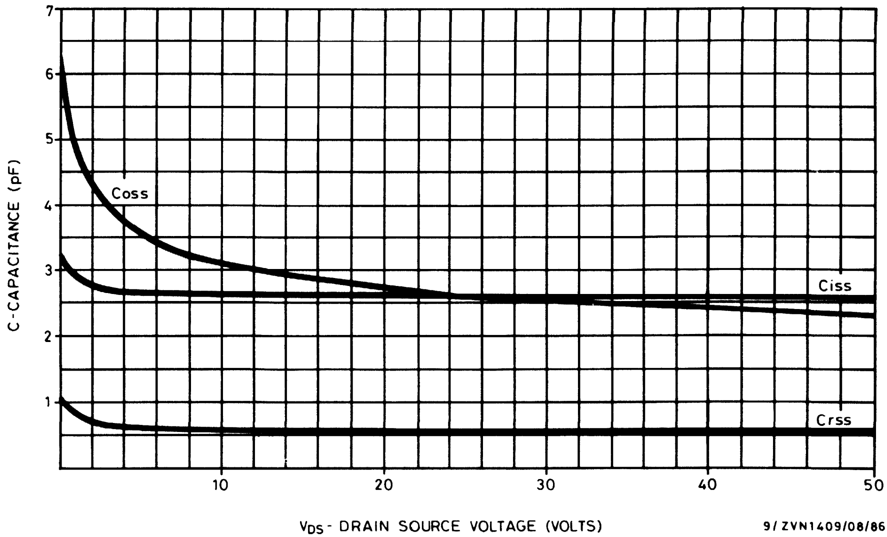


Fig. 9 Typical capacitance v drain-source voltage

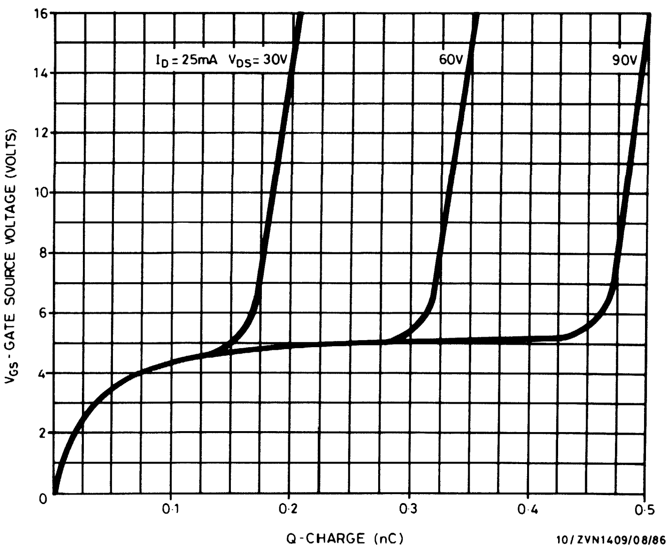


Fig. 10 Typical gate charge v gate-source voltage

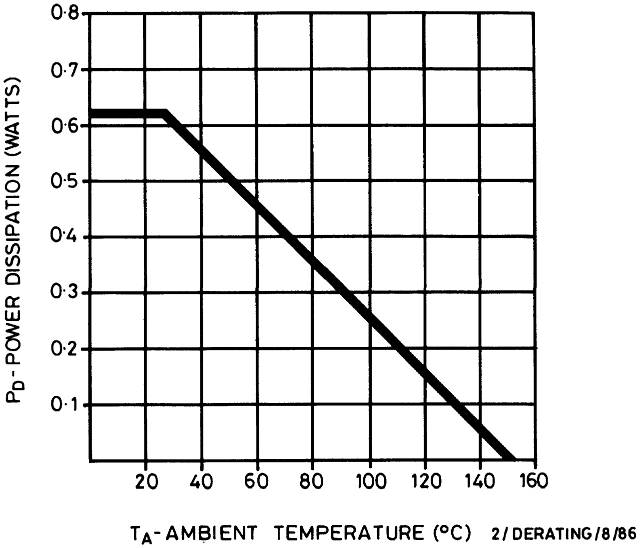


Fig. 11 Power v temperature derating curve (ambient)

N-channel enhancement mode vertical DMOS FET

ZVN2106

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

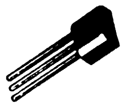
DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

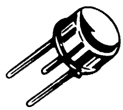
PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2106A*	60V	0.45A	2Ω
ZVN2106B*	60V	1.2A	2Ω
ZVN2106L	60V	2.0A	2Ω

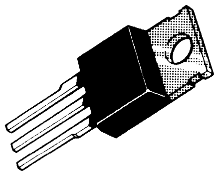
*BS-CECC approved.



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVN2106

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	60	60	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.45	0.45	0.65	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	1.2	2	A
I_{DM}	Pulse drain current	8	8	8	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	0.5	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	0.1	mA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	2	3	–	A	$V_{DS} = 18V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	2	Ω	$I_D = 1A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	0.3	0.4	–	S	$V_{DS} = 18V$, $I_D = 1A$
C_{iss}	Input capacitance (2)	–	60	75	pF	$V_{DS} = 18V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	30	45	pF	
C_{rss}	Reverse transfer capacitance (2)	–	15	20	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	4	7	ns	$V_{DD} \approx 18V$, $I_D = 1A$
t_r	Rise time (2) (3)	–	5	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	12	ns	
t_f	Fall time (2) (3)	–	10	15	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.82	V	$V_{GS}=0V$, $I_S=0.45A$
t_{rr}	Reverse recovery time	50	ns	$V_{GS}=0V$, $I_F=0.45A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

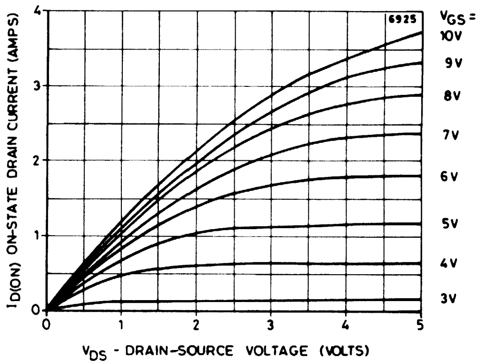


Fig. 1 Typical saturation characteristics

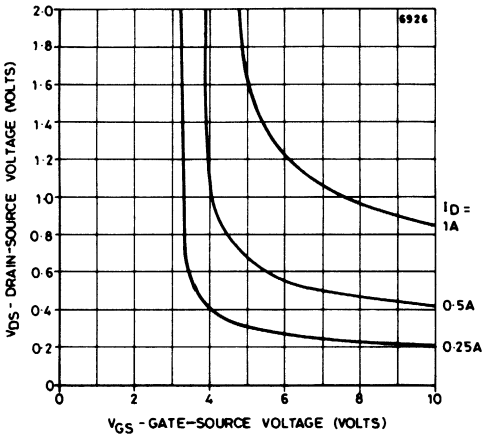


Fig. 2 Typical voltage saturation characteristics

ZVN2106

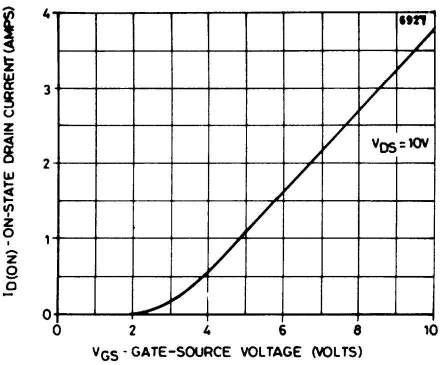


Fig. 3 Typical transfer characteristics

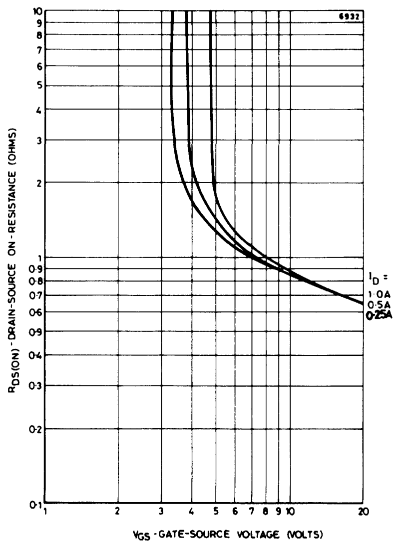


Fig. 4 Typical on-resistance v gate-source voltage

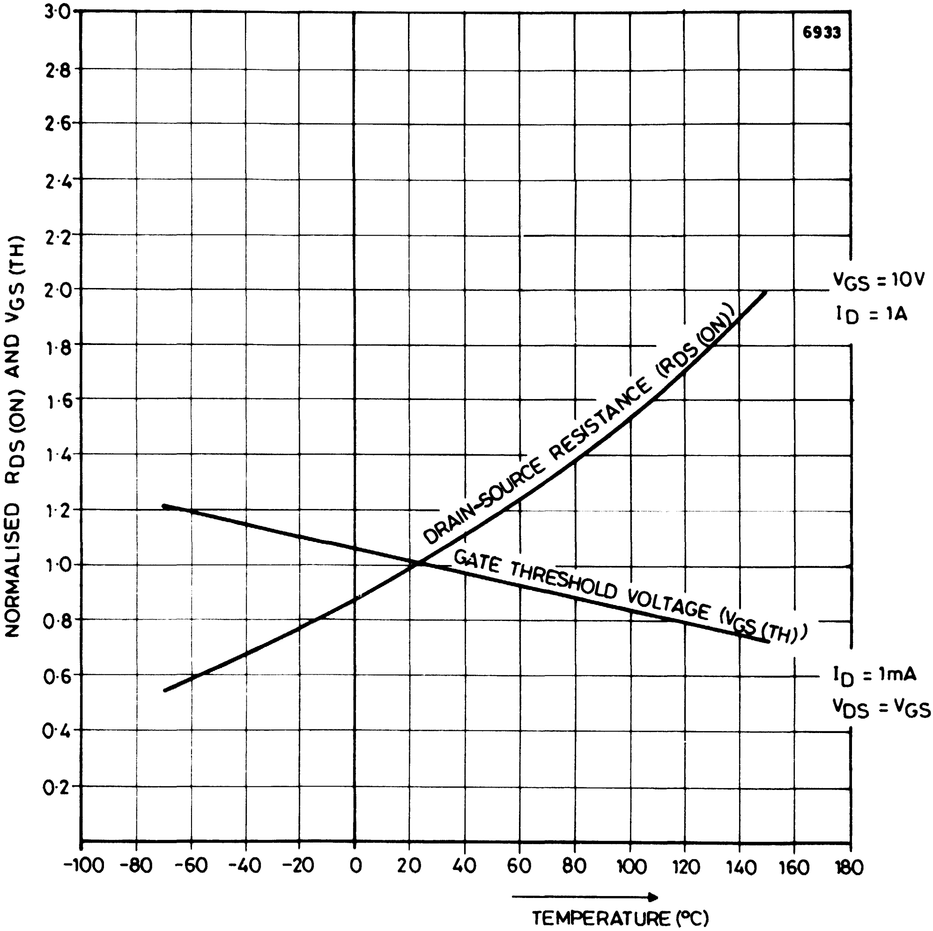


Fig. 5 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

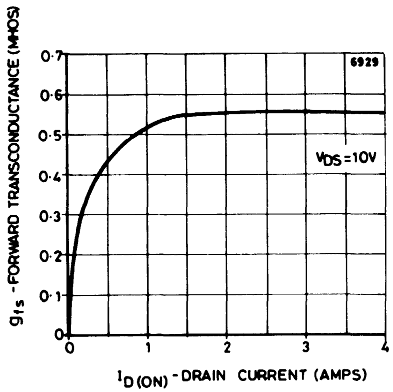


Fig. 6 Typical transconductance v drain current

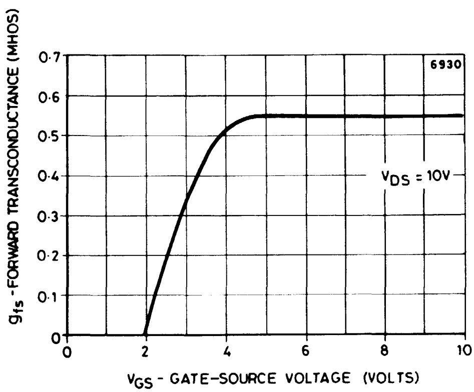


Fig. 7 Typical transconductance v gate-source voltage

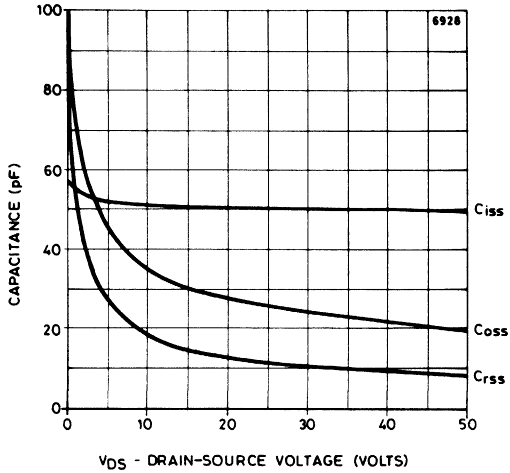


Fig. 8 Typical capacitance v drain-source voltage

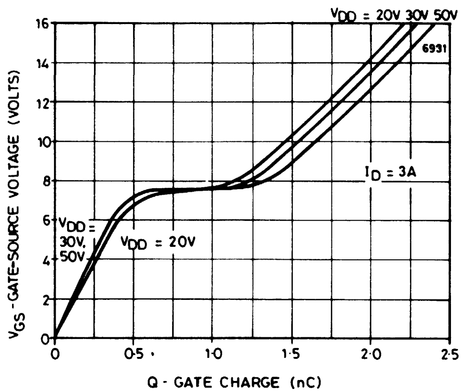


Fig. 9 Typical gate charge v gate-source voltage

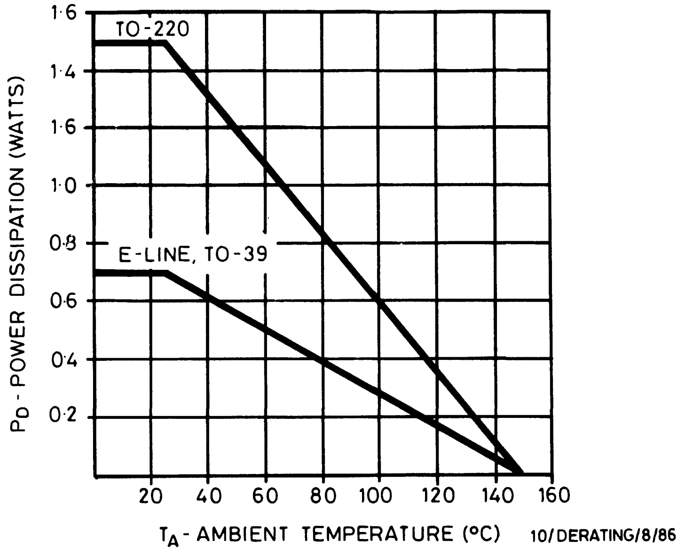


Fig. 10 Power v temperature derating curve (ambient)

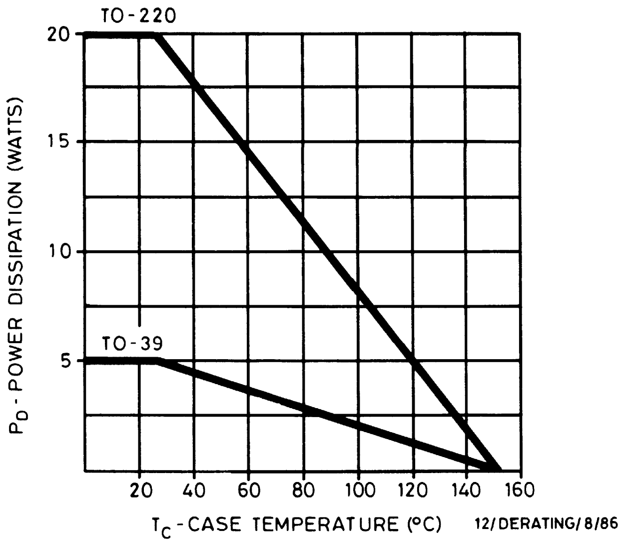


Fig. 11 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

ZVN2110

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

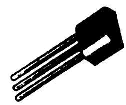
DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

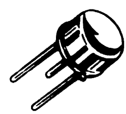
PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2110A*	100V	0.32A	4Ω
ZVN2110B*	100V	0.85A	4Ω
ZVN2110L	100V	1.5A	4Ω

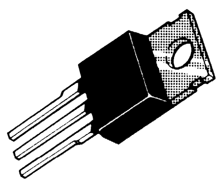
*BS-CECC approved.



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVN2110

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	100	100	100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.32	0.32	0.46	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.85	1.5	A
I_{DM}	Pulse drain current	6	6	6	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	100	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	1	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	1.5	2	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	4	Ω	$I_D = 1A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	250	350	–	mS	$V_{DS} = 25V$, $I_D = 1A$
C_{iss}	Input capacitance (2)	–	59	75	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	16	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	8	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	4	7	ns	$V_{DD} \approx 25V$, $I_D = 1A$
t_r	Rise time (2) (3)	–	4	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	13	ns	
t_f	Fall time (2) (3)	–	8	13	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.82	V	$V_{GS}=0V$, $I_S=0.32A$
t_{rr}	Reverse recovery time	112	ns	$V_{GS}=0V$, $I_F=0.32A$ $I_R=0.1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

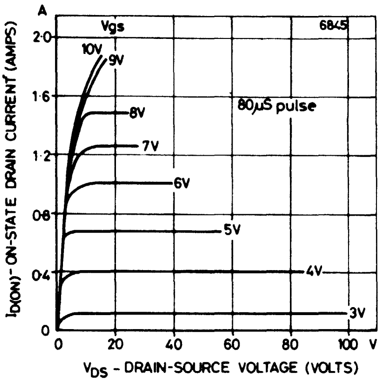


Fig. 1 Typical output characteristics

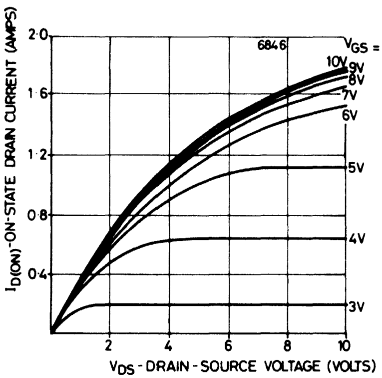


Fig. 2 Typical saturation characteristics

ZVN2110

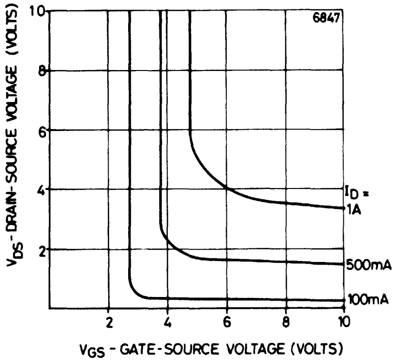


Fig. 3 Typical voltage saturation characteristics

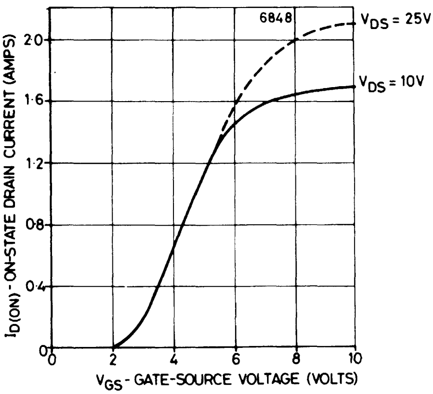


Fig. 4 Typical transfer characteristics

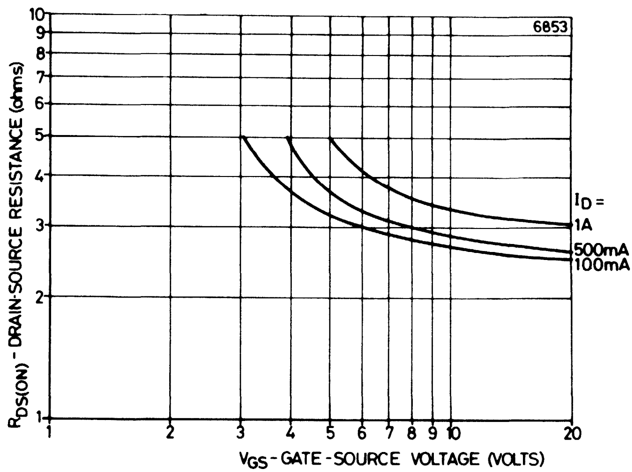


Fig. 5 Typical on-resistance v gate-source voltage

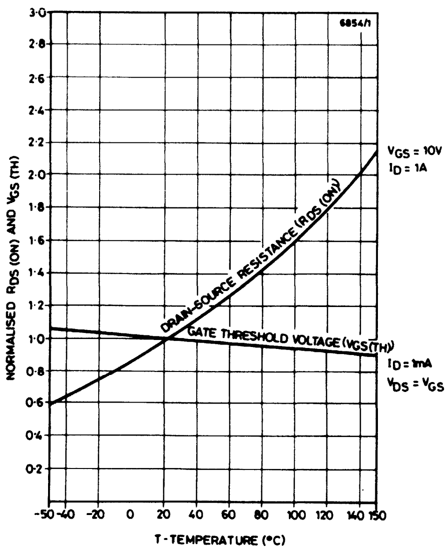


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

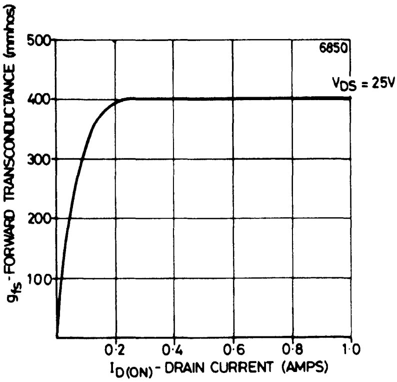


Fig. 7 Typical transconductance v drain current

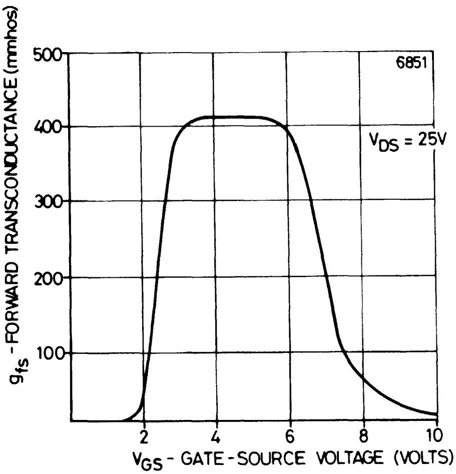


Fig. 8 Typical transconductance v gate-source voltage

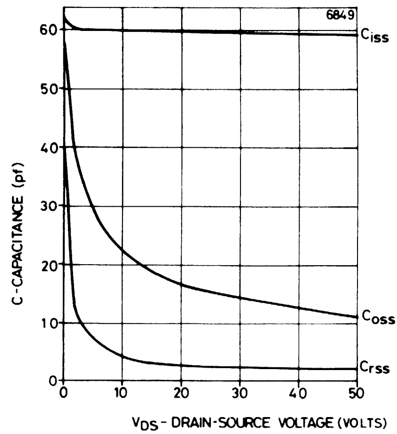


Fig. 9 Typical capacitance v drain-source voltage

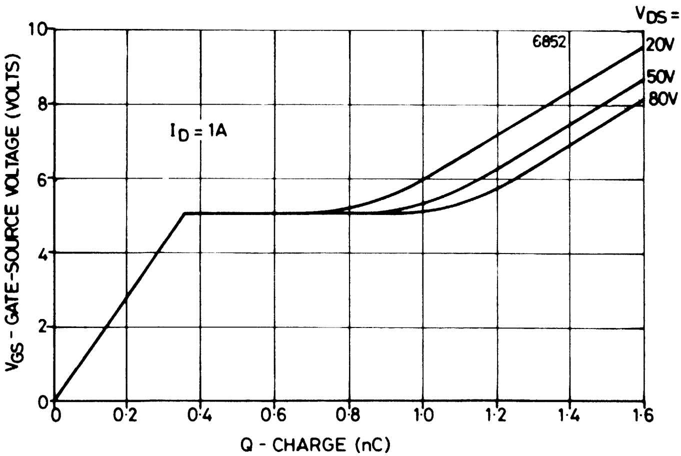


Fig. 10 Typical gate charge v gate-source voltage

ZVN2110

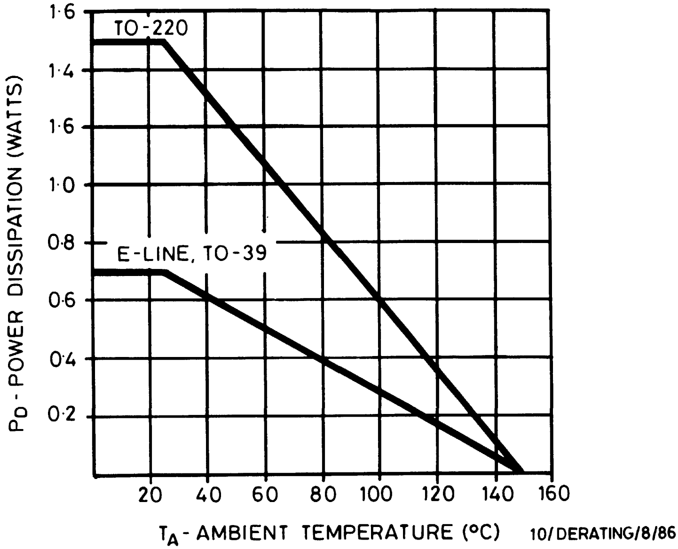


Fig. 11 Power v temperature derating curve (ambient)

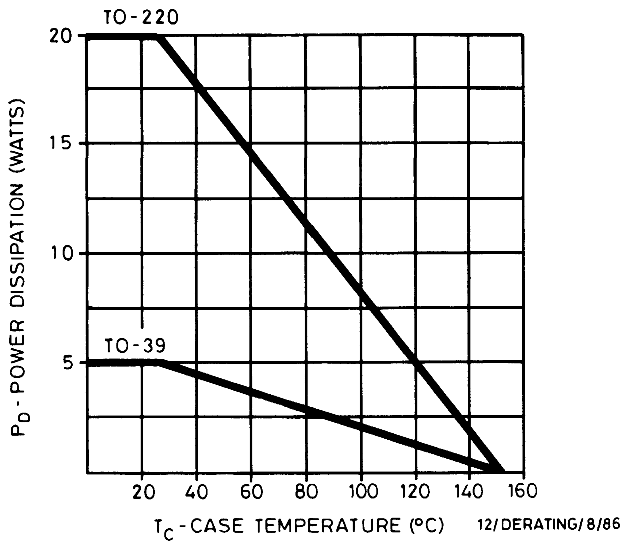


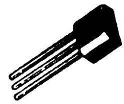
Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

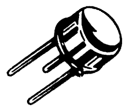
ZVN2120

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



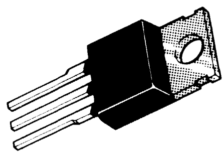
E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.



TO-220
SUFFIX L

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2120A	200V	0.18A	10Ω
ZVN2120B	200V	0.46A	10Ω
ZVN2120L	200V	0.5A	10Ω

ZVN2120

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	200	200	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.18	0.18	0.27	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.46	0.50	A
I_{DM}	Pulse drain current	2	2	2	A
V_{GS}	Gate-source voltage	± 20	± 20	± 20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at $T = 25°C$ unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	500	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	10	Ω	$I_D = 250mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 250mA$
C_{iss}	Input capacitance (2)	–	85	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx 25V$, $I_D = 250mA$
t_r	Rise time (2) (3)	–	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	20	ns	
t_f	Fall time (2) (3)	–	12	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle $\leqslant$2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

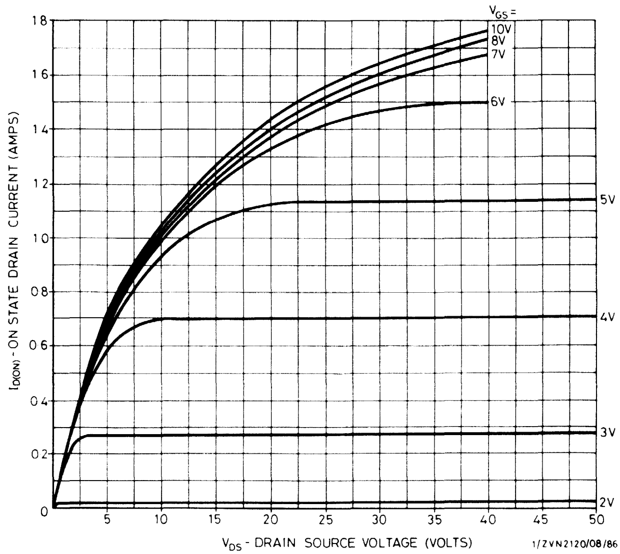


Fig. 1 Typical output characteristics

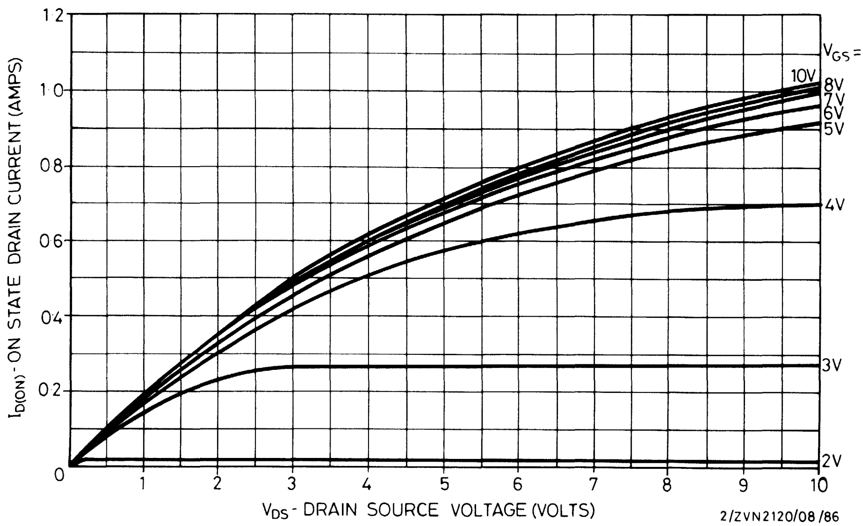


Fig. 2 Typical saturation characteristics

ZVN2120

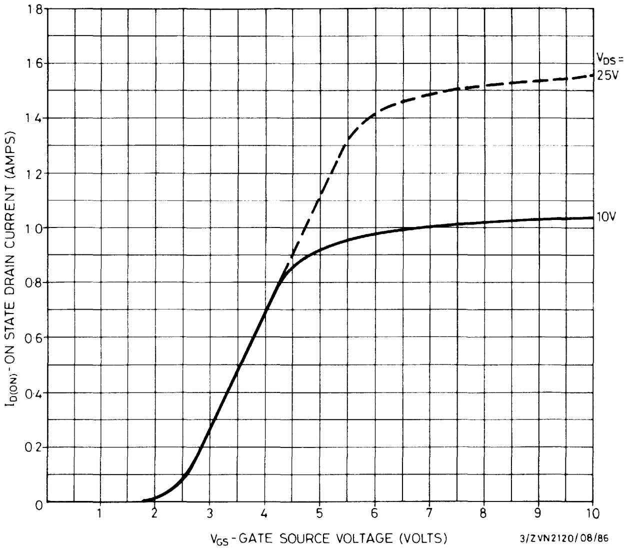


Fig. 3 Typical transfer characteristics

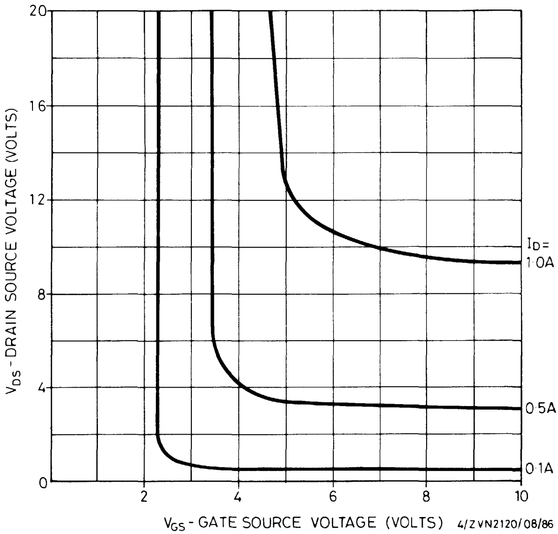


Fig. 4 Typical voltage saturation characteristics

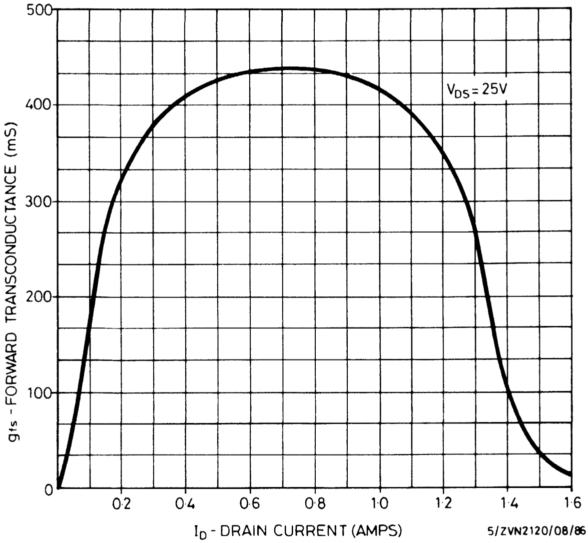


Fig. 5 Typical transconductance v drain current

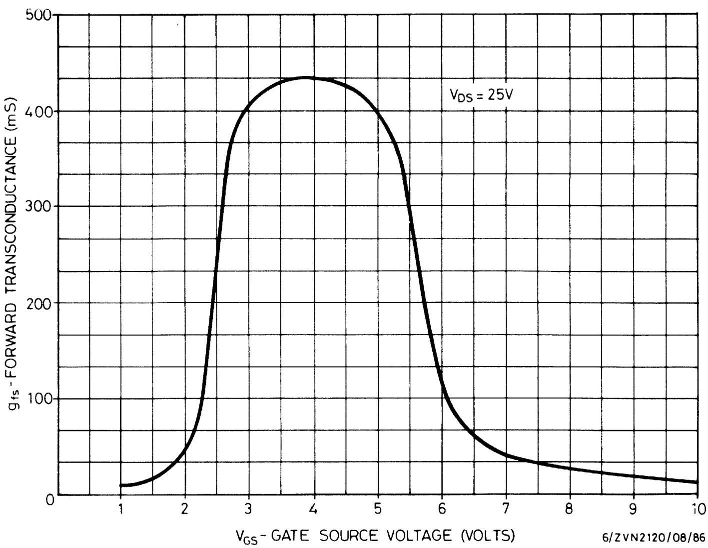


Fig. 6 Typical transconductance v gate-source voltage

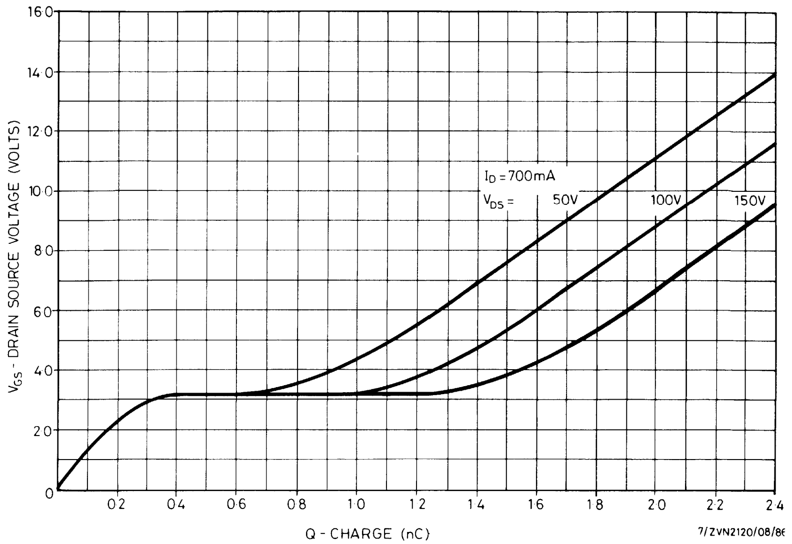


Fig. 7 Typical gate charge v gate-source voltage

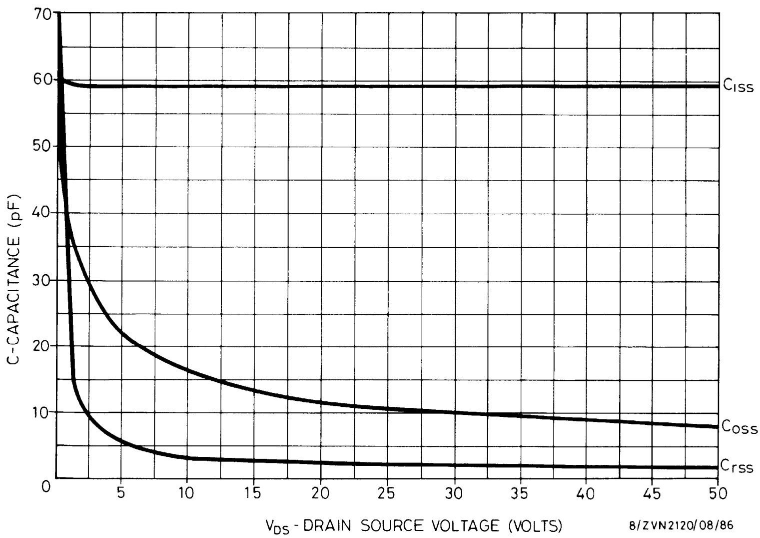


Fig. 8 Typical capacitance v drain-source voltage

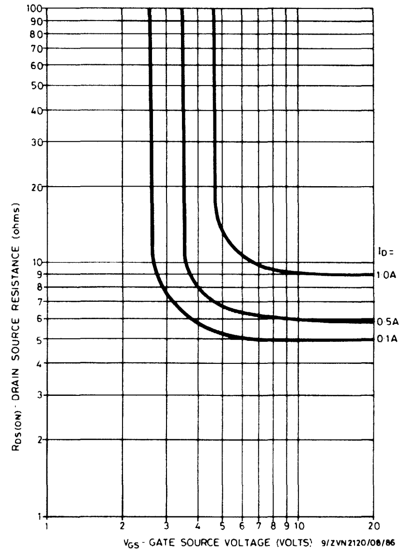


Fig. 9 Typical on-resistance v gate-source voltage

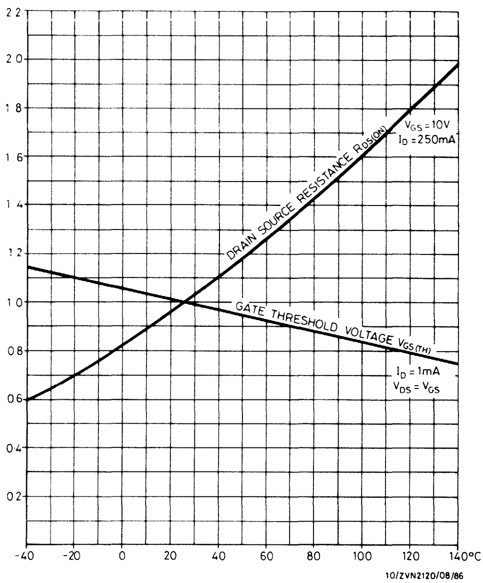


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

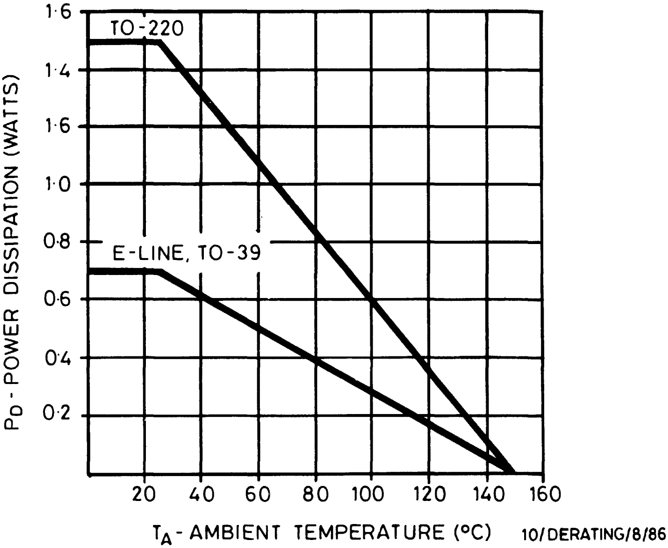


Fig. 11 Power v temperature derating curve (ambient)

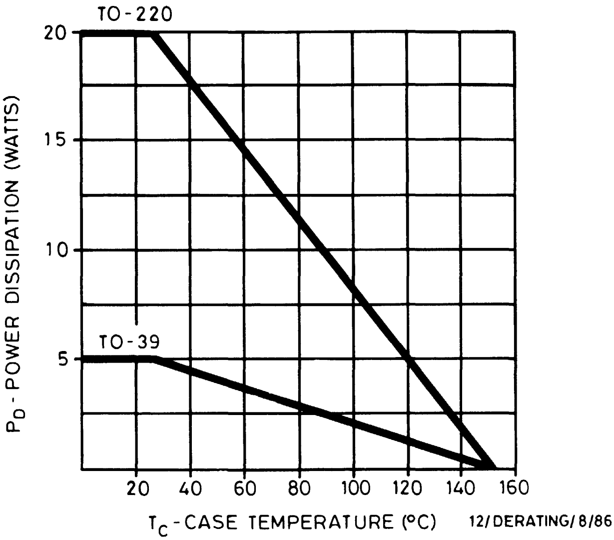


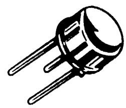
Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

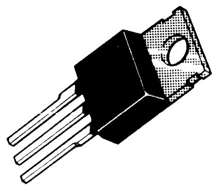
ZVN2206

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-39
SUFFIX B



TO-220
SUFFIX L

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2206B*	60V	4.8A	0.5Ω
ZVN2206L	60V	4.8A	0.5Ω

*BS-CECC approved

ZVN2206

ABSOLUTE MAXIMUM RATINGS

	Parameters	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	60	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.9	1.3	A
I_D	Continuous drain current (@ $T_C = 25°C$)	4.8	4.8	A
I_{DM}	Pulse drain current	16	16	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	20	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	–	V	$I_D = 10\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	–	3	V	$I_D = 2mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	2	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	200	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	4	8	–	A	$V_{DS} = 18V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	0.5	Ω	$I_D = 2A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	–	1.4	–	S	$V_{DS} = 18V$, $I_D = 2A$
C_{iss}	Input capacitance (2)	–	170	220	pF	$V_{DS} = 18V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	80	100	pF	
C_{rss}	Reverse transfer capacitance (2)	–	35	80	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3.7	5	ns	$V_{DD} \approx 18V$, $I_D = 2A$
t_r	Rise time (2) (3)	–	14	20	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	17	26	ns	
t_f	Fall time (2) (3)	–	18	25	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.95	V	$V_{GS}=0V$, $I_S=4A$
t_{rr}	Reverse recovery time	59	ns	$V_{GS}=0V$, $I_F=4A$ $I_R=1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

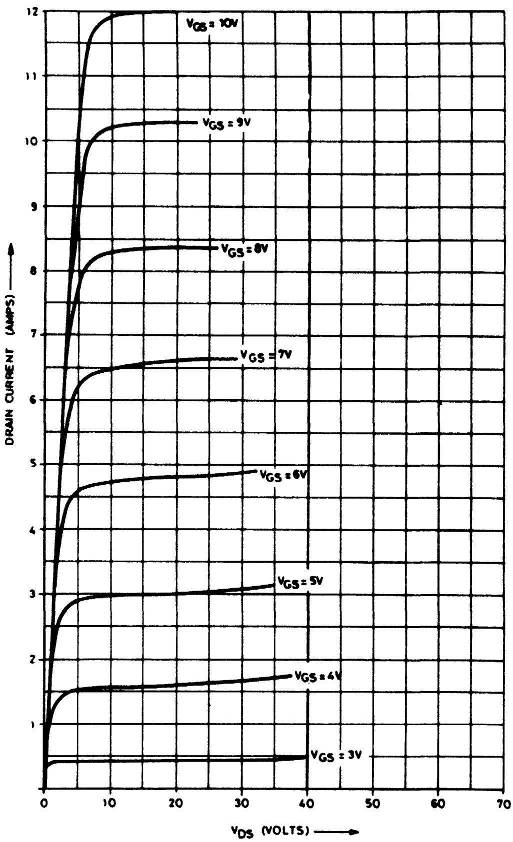


Fig. 1 Typical output characteristics

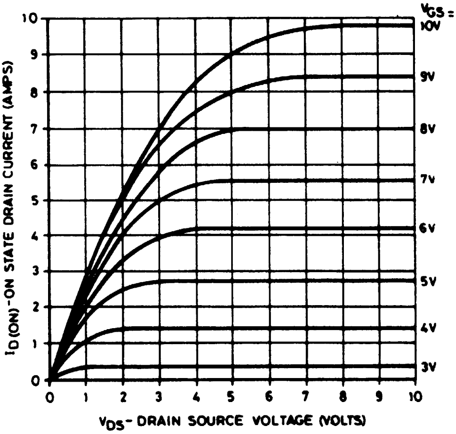


Fig. 2 Typical saturation characteristics

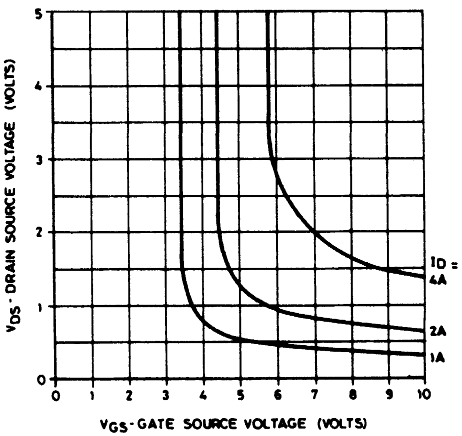


Fig. 3 Typical voltage saturation characteristics

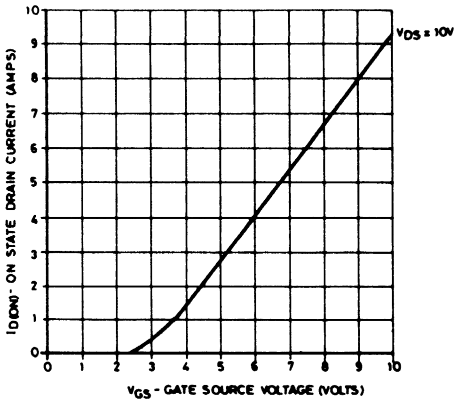


Fig. 4 Typical transfer characteristics

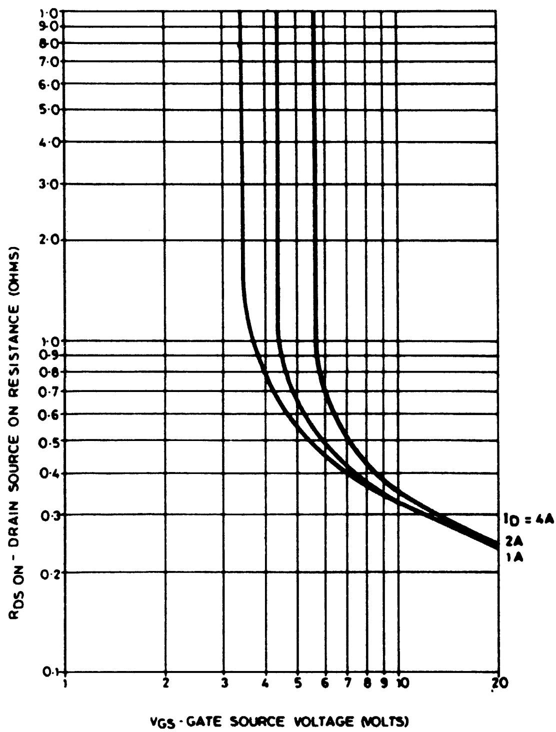


Fig. 5 Typical on-resistance v gate-source voltage

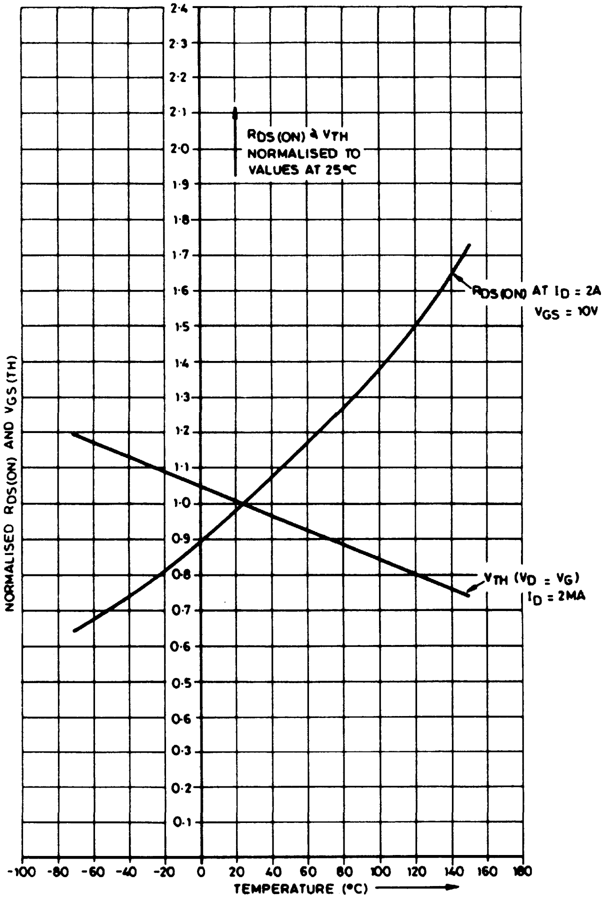


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

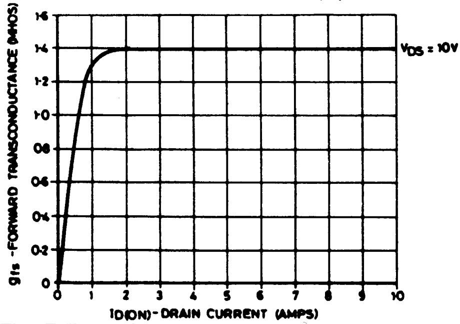


Fig. 7 Typical transconductance v drain current

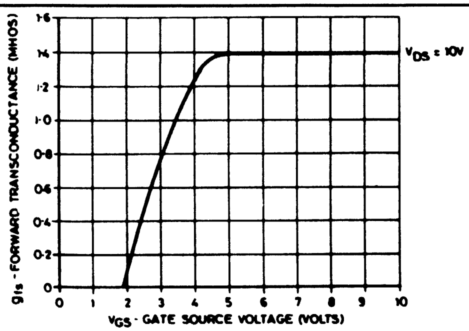


Fig. 8 Typical transconductance v gate-source voltage

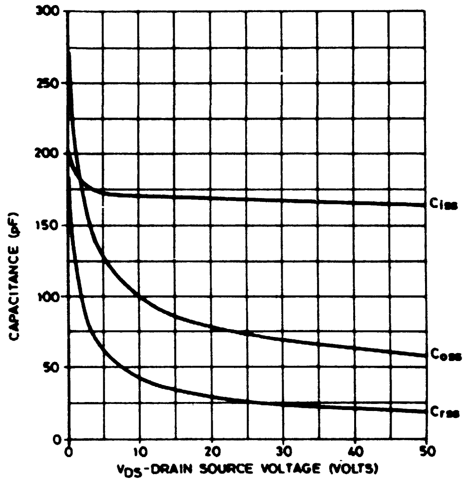


Fig. 9 Typical capacitance v drain-source voltage

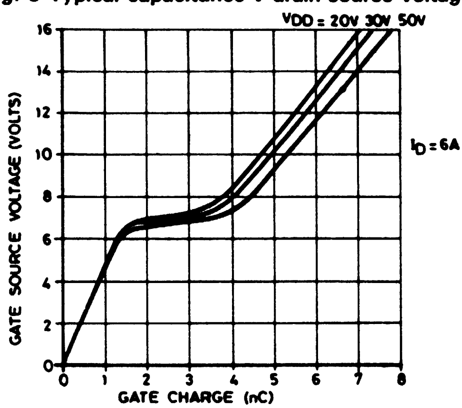


Fig. 10 Typical gate charge v gate-source voltage

ZVN2206

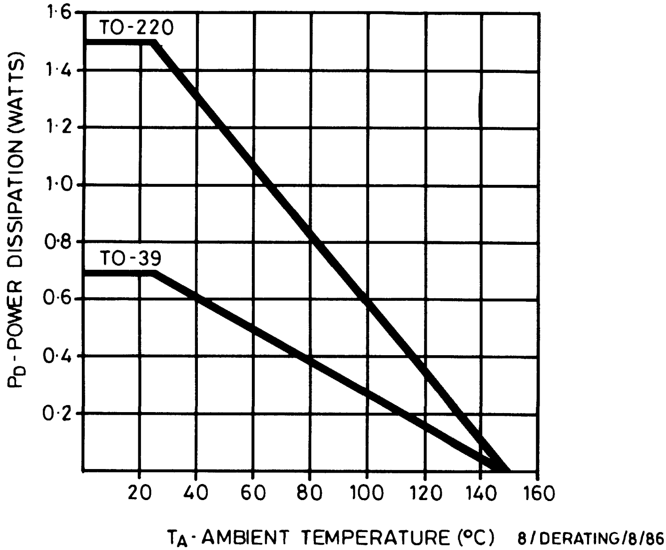


Fig. 11 Power v temperature derating curve (ambient)

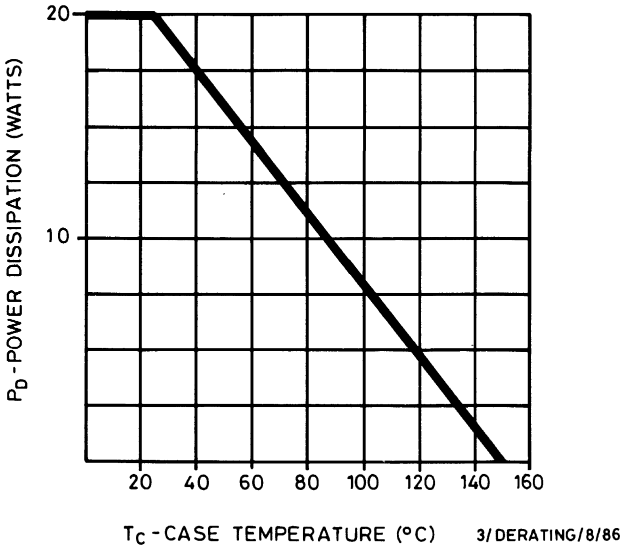


Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

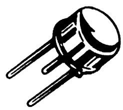
ZVN2210

FEATURES

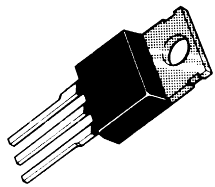
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.



TO-39
SUFFIX B



TO-220
SUFFIX L

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2210B*	100V	3.45A	0.8Ω
ZVN2210L	100V	3.45A	0.8Ω

*BS-CECC approved

ZVN2210

ABSOLUTE MAXIMUM RATINGS

Parameters		TO-39	T0-220	Units
V_{DS}	Drain-source voltage	100	100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.65	0.95	A
I_D	Continuous drain current (@ $T_C = 25°C$)	3.45	3.45	A
I_{DM}	Pulse drain current	12	12	A
V_{GS}	Gate-source voltage	± 20	± 20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	20	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at $T = 25°C$ unless otherwise stated)

Parameter		Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	100	–	–	V	$I_D = 10\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	–	3	V	$I_D = 2mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	2	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	200	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	3	6	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	0.8	Ω	$I_D = 2A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	–	1.2	–	S	$V_{DS} = 25V$, $I_D = 1.5A$
C_{iss}	Input capacitance (2)	–	160	220	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	50	75	pF	
C_{rss}	Reverse transfer capacitance (2)	–	16	25	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3.3	5	ns	$V_{DD} \approx 25V$, $I_D = 2A$
t_r	Rise time (2) (3)	–	15	25	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	17	26	ns	
t_f	Fall time (2) (3)	–	15	25	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.89	V	$V_{GS}=0V$, $I_S=3A$
t_{rr}	Reverse recovery time	124	ns	$V_{GS}=0V$, $I_F=3A$ $I_R=1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

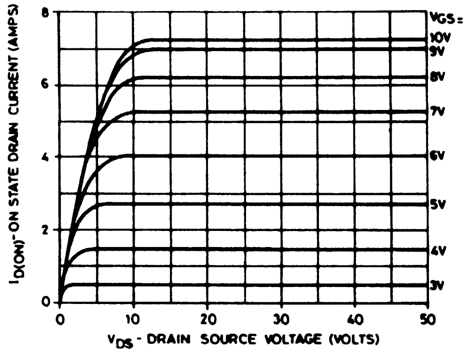


Fig. 1 Typical output characteristics

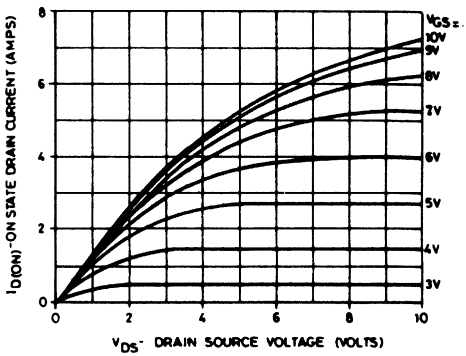


Fig. 2 Typical saturation characteristics

ZVN2210

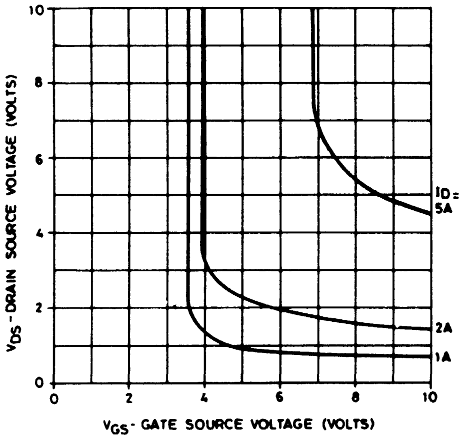


Fig. 3 Typical voltage saturation characteristics

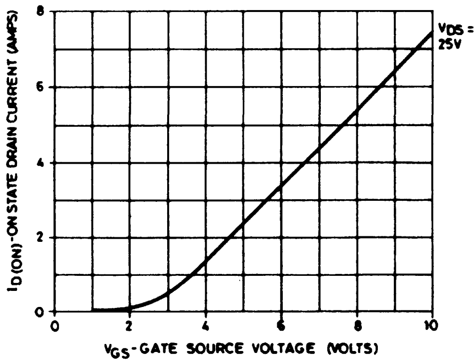


Fig. 4 Typical transfer characteristics

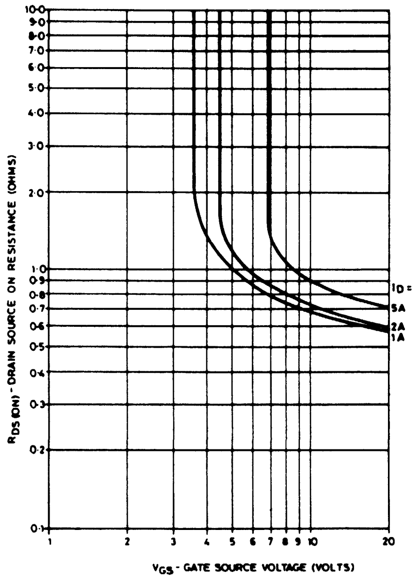


Fig. 5 Typical on-resistance v gate-source voltage

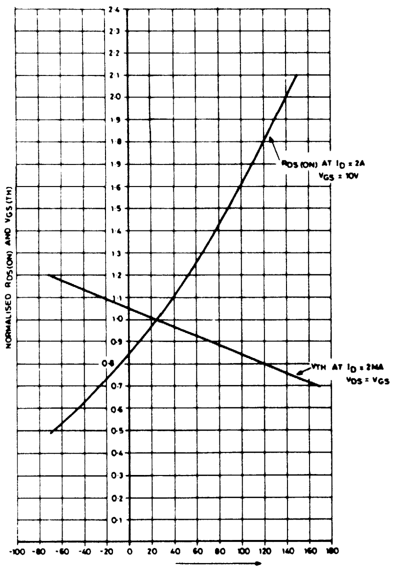


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

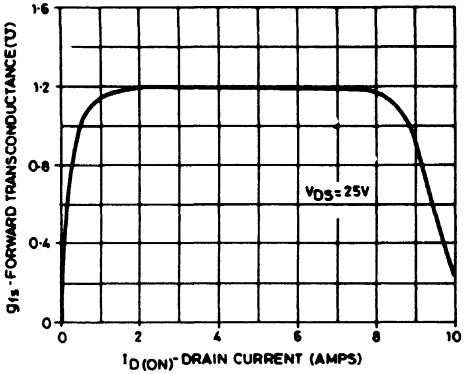


Fig. 7 Typical transconductance v drain current

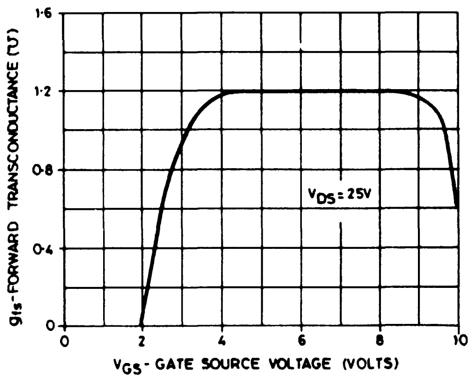


Fig. 8 Typical transconductance v gate-source voltage

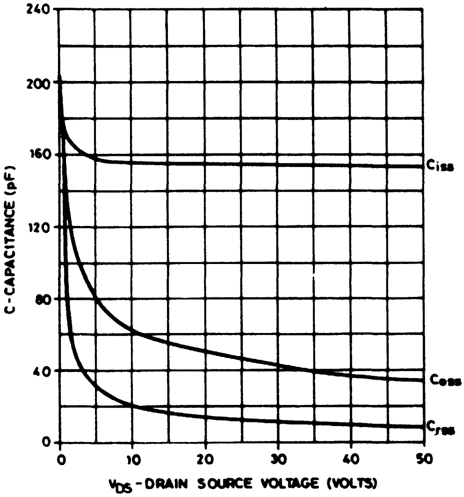


Fig. 9 Typical capacitance v drain-source voltage

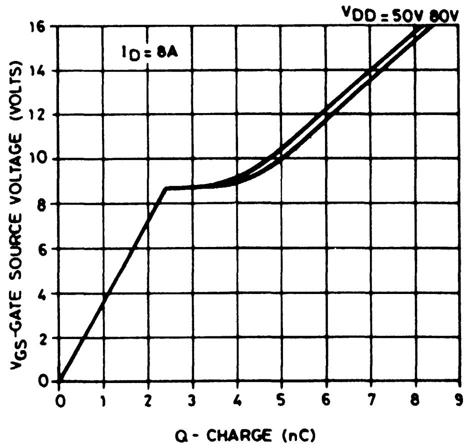


Fig. 10 Typical gate charge v gate-source voltage

ZVN2210

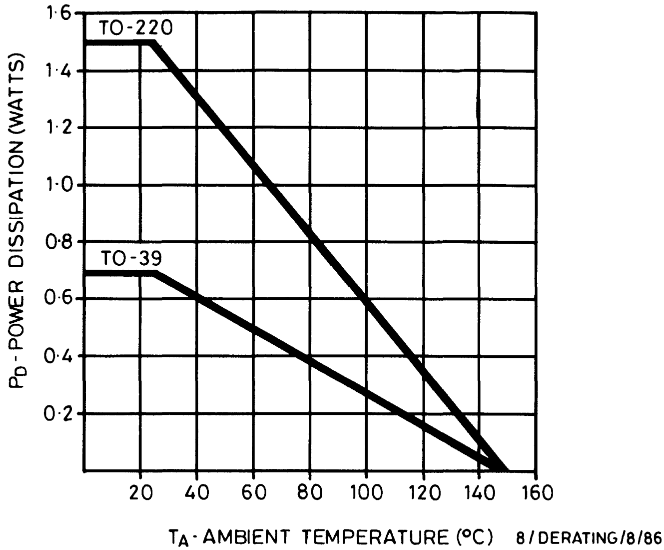


Fig. 11 Power v temperature derating curve (ambient)

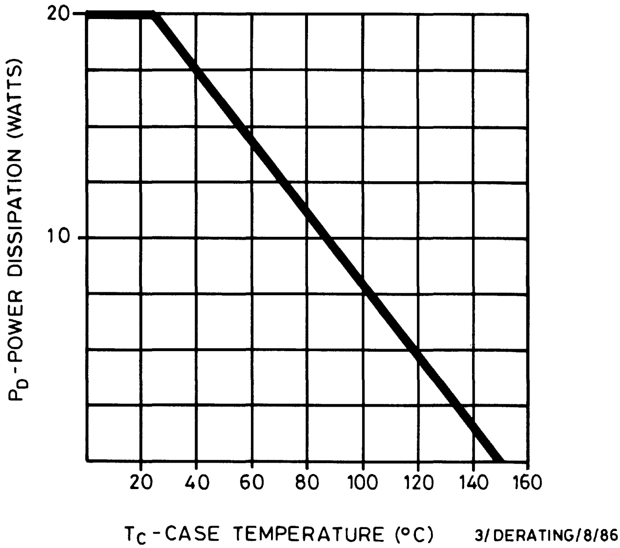


Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

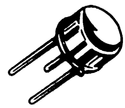
ZVN2220

FEATURES

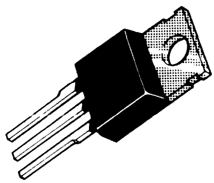
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.



TO-39
SUFFIX B



TO-220
SUFFIX L

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2220B	200V	1.85A	2.5Ω
ZVN2220L	200V	1.85A	2.5Ω

ZVN2220

ABSOLUTE MAXIMUM RATINGS

	Parameters	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	200	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.35	0.5	A
I_D	Continuous drain current (@ $T_C = 25°C$)	1.85	1.85	A
I_{DM}	Pulse drain current	8	8	A
V_{GS}	Gate-source voltage	± 20	± 20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	20	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	–	–	V	$I_D = 10\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	–	3	V	$I_D = 2mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	1	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	200	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	2	3	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	2.5	Ω	$I_D = 1A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	–	1	–	S	$V_{DS} = 25V$, $I_D = 1A$
C_{iss}	Input capacitance (2)	–	170	220	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	30	45	pF	
C_{rss}	Reverse transfer capacitance (2)	–	6	10	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3	6	ns	$V_{DD} \approx 25V$, $I_D = 1A$
t_r	Rise time (2) (3)	–	6	10	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	20	26	ns	
t_f	Fall time (2) (3)	–	11	15	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.85	V	$V_{GS}=0V$, $I_S=2A$
t_{rr}	Reverse recovery time	175	ns	$V_{GS}=0V$, $I_F=2A$ $I_R=1A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle $\leqslant$ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

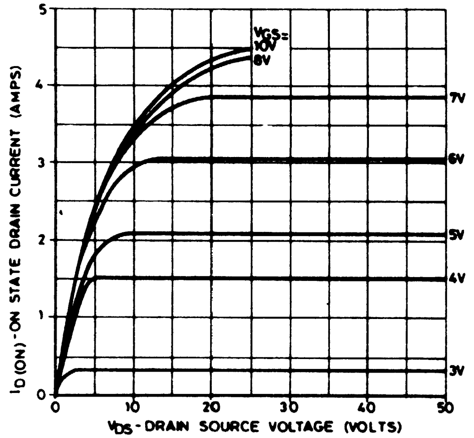


Fig. 1 Typical output characteristics

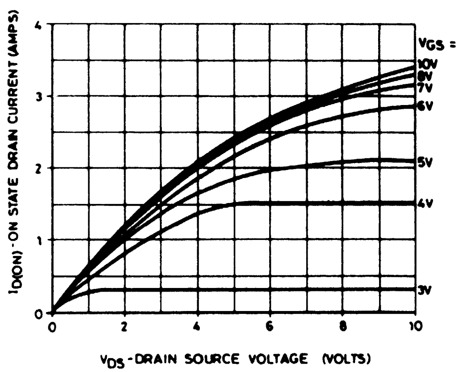


Fig. 2 Typical saturation characteristics

ZVN2220

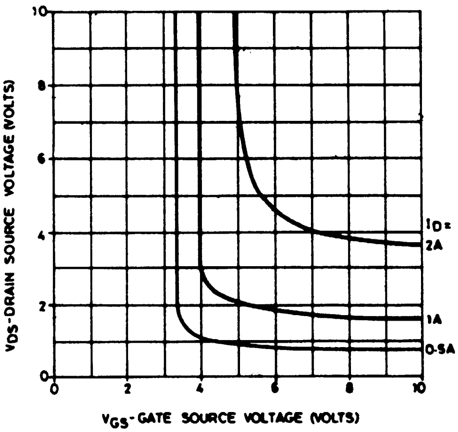


Fig. 3 Typical voltage saturation characteristics

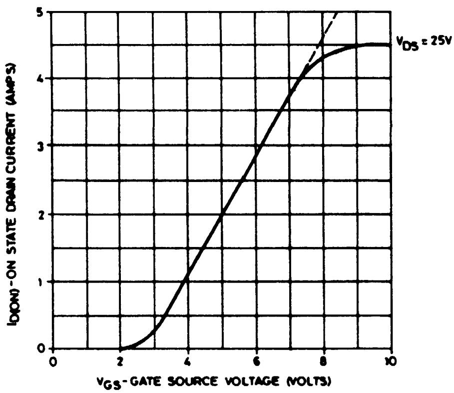


Fig. 4 Typical transfer characteristics

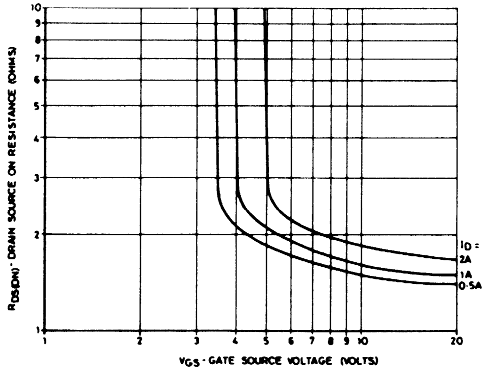


Fig. 5 Typical on-resistance v gate-source voltage

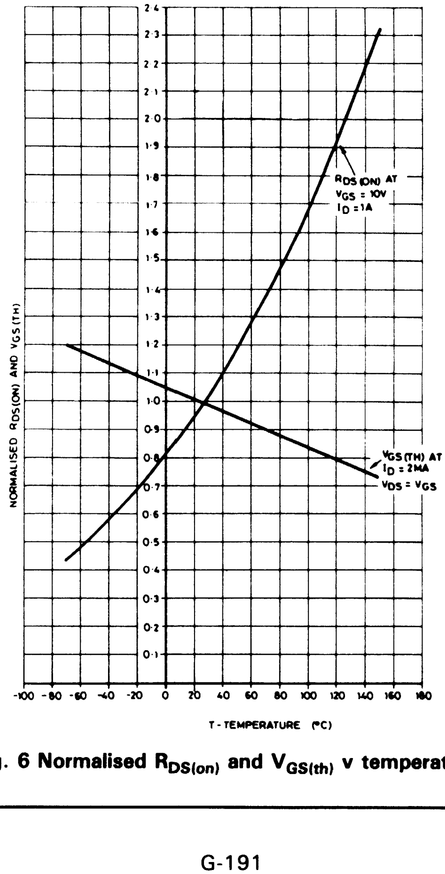


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

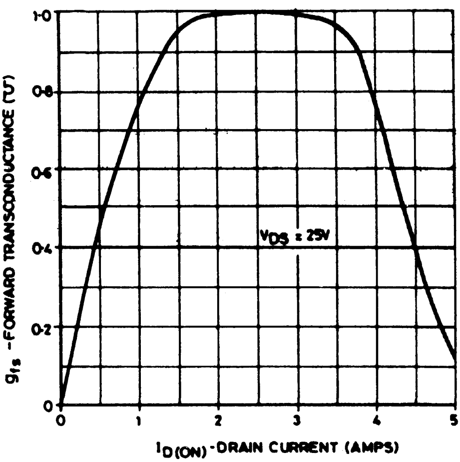


Fig. 7 Typical transconductance v drain current

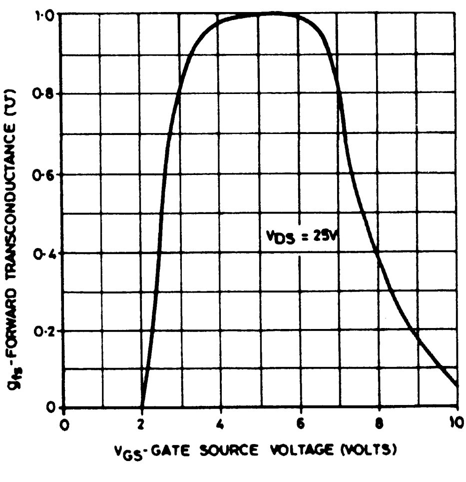


Fig. 8 Typical transconductance v gate-source voltage

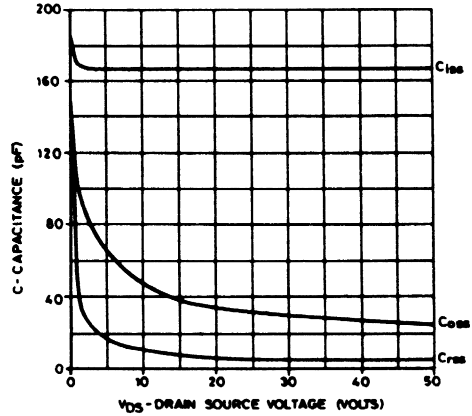


Fig. 9 Typical capacitance v drain-source voltage

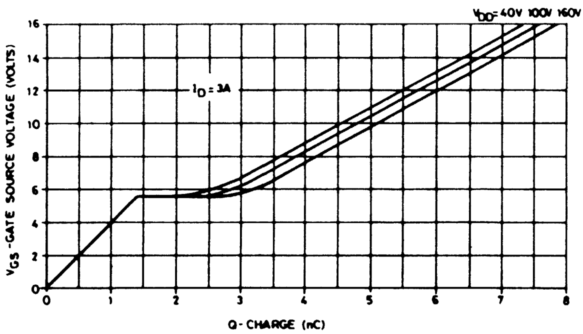


Fig. 10 Typical gate charge v gate-source voltage

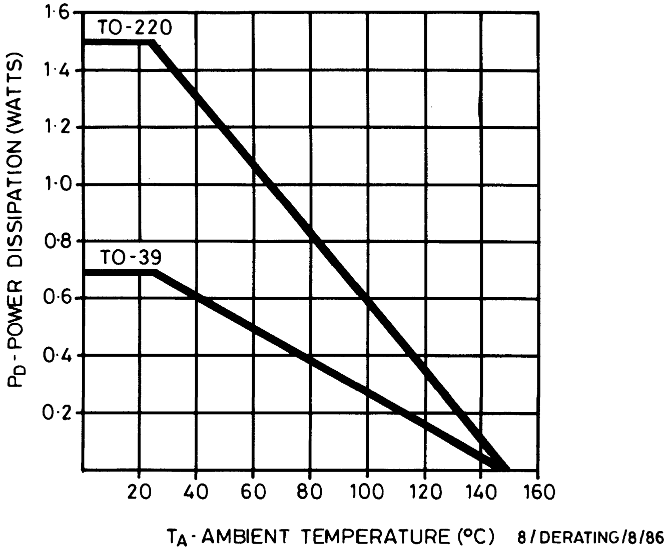


Fig. 11 Power v temperature derating curve (ambient)

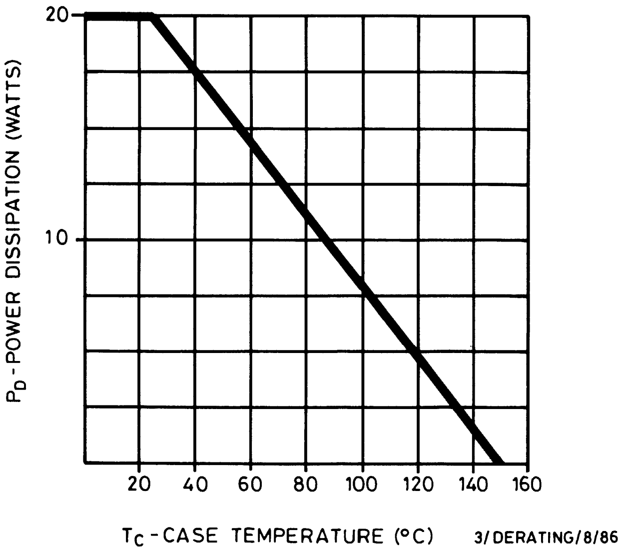


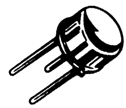
Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

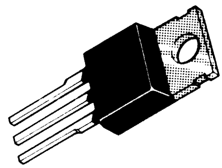
ZVN2224

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-39
SUFFIX B



TO-220
SUFFIX L

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2224B	240V	1.2A	6Ω
ZVN2224L	240V	1.2A	6Ω

ZVN2224

ABSOLUTE MAXIMUM RATINGS

	Parameters	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	240	240	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.23	0.33	A
I_D	Continuous drain current (@ $T_C = 25°C$)	1.2	1.2	A
I_{DM}	Pulse drain current	6	6	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	20	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	240	–	–	V	$I_D = 10\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	–	3	V	$I_D = 2mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	200	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	1.5	2	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	4	6	Ω	$I_D = 1A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	–	750	–	mS	$V_{DS} = 25V$, $I_D = 1A$
C_{iss}	Input capacitance (2)	–	–	220	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	–	45	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	10	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	–	6	ns	$V_{DD} \approx 25V$, $I_D = 1A$
t_r	Rise time (2) (3)	–	–	10	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	–	26	ns	
t_f	Fall time (2) (3)	–	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement mode vertical DMOS FET

ZVN2535

FEATURES

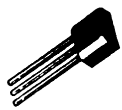
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

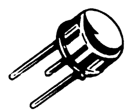
A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

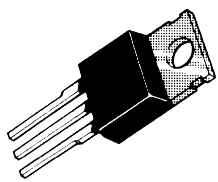
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN2535A	350V	0.09A	35Ω
ZVN2535B	350V	0.25A	35Ω
ZVN2535L	350V	0.25A	35Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVN2535

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	350	350	350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.09	0.09	0.14	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.25	0.25	A
I_{DM}	Pulse drain current	1	1	1	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	350	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	400	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	250	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	35	Ω	$I_D = 100mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	70	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	10	pF	
C_{rss}	Reverse transfer capacitance (2)	–	4	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx 25V$, $I_D = 100mA$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	16	ns	
t_f	Fall time (2) (3)	–	10	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

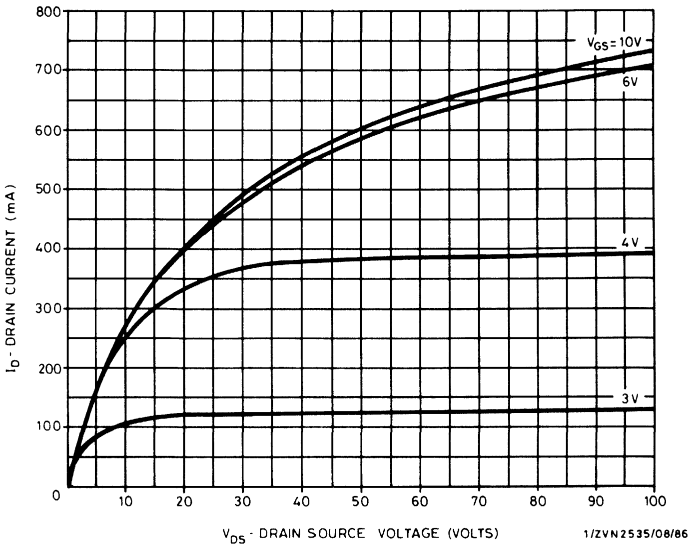


Fig. 1 Typical output characteristics

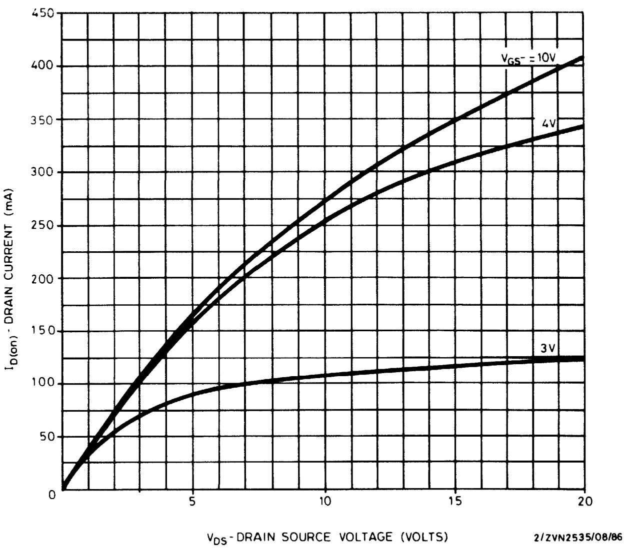


Fig. 2 Typical saturation characteristics

ZVN2535

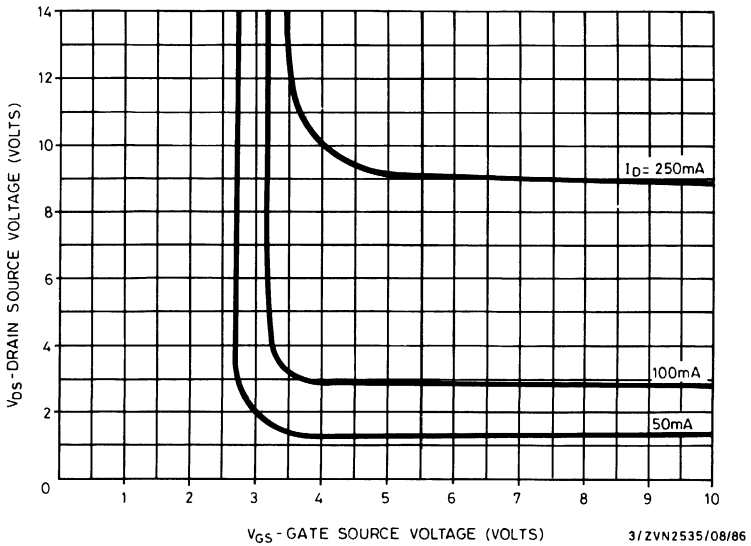


Fig. 3 Typical voltage saturation characteristics

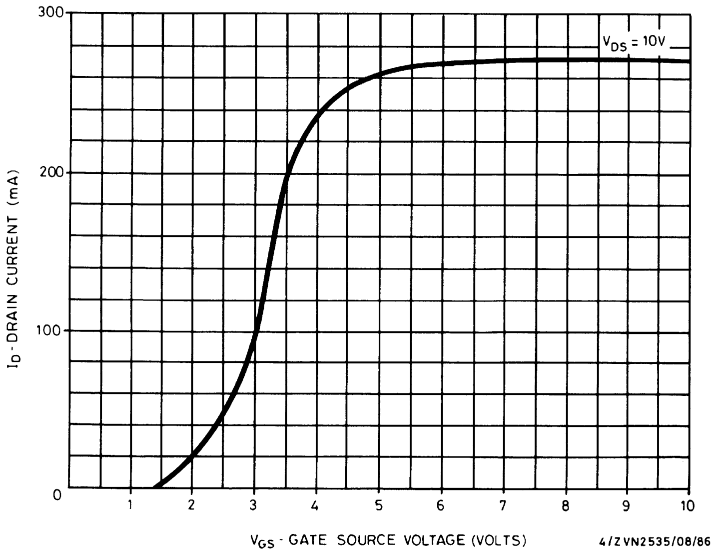


Fig. 4 Typical transfer characteristics

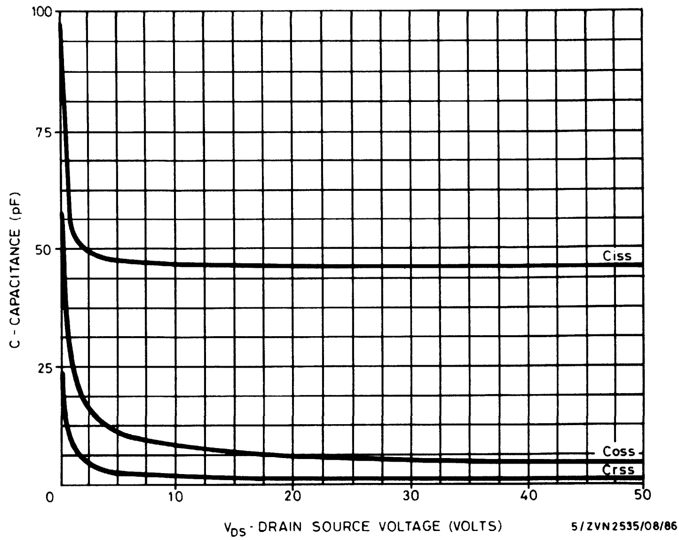


Fig. 5 Typical capacitance v drain-source voltage

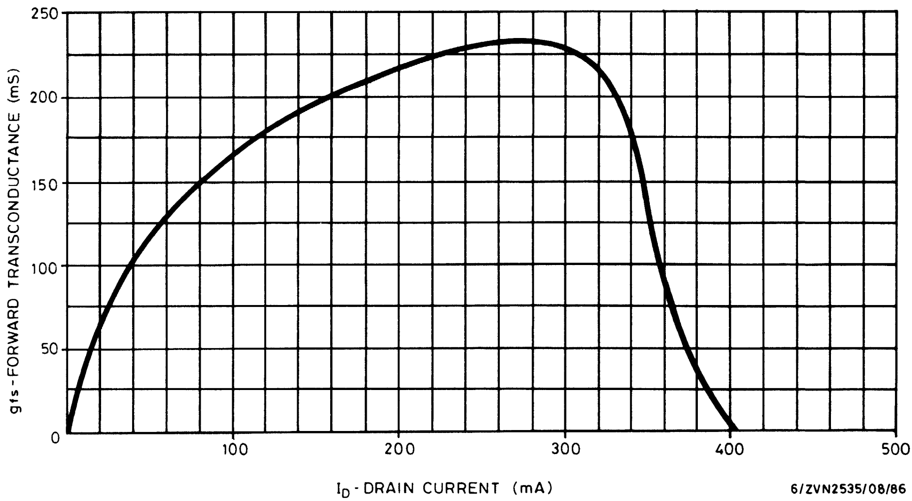


Fig. 6 Typical transconductance v drain current

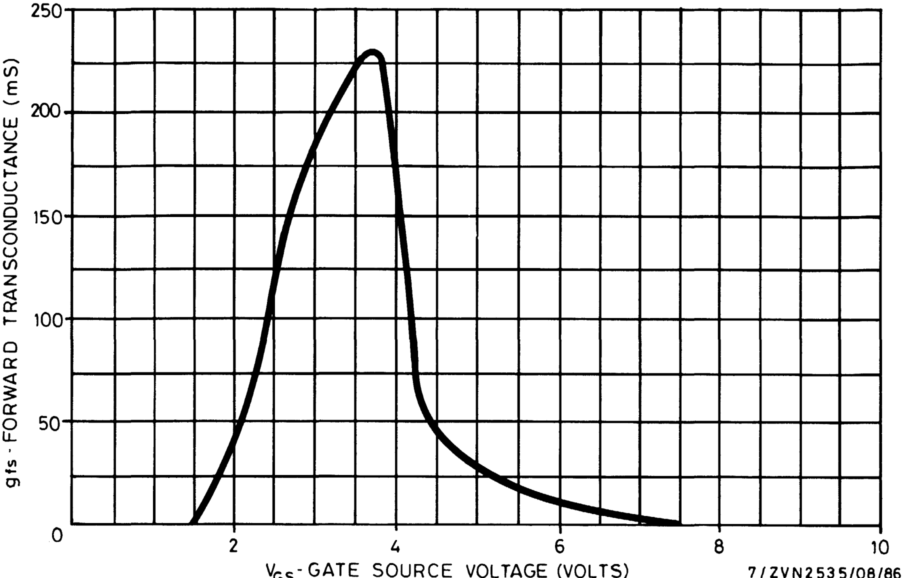


Fig. 7 Typical transconductance v gate-source voltage

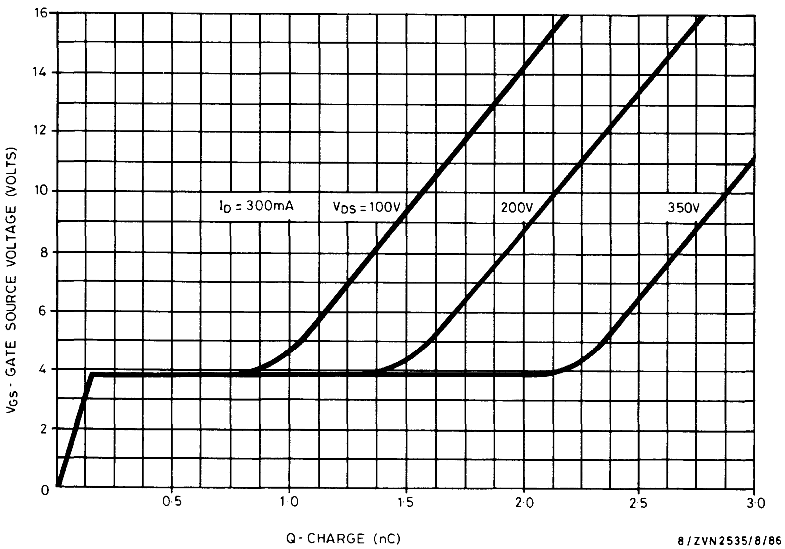


Fig. 8 Typical gate charge v gate-source voltage

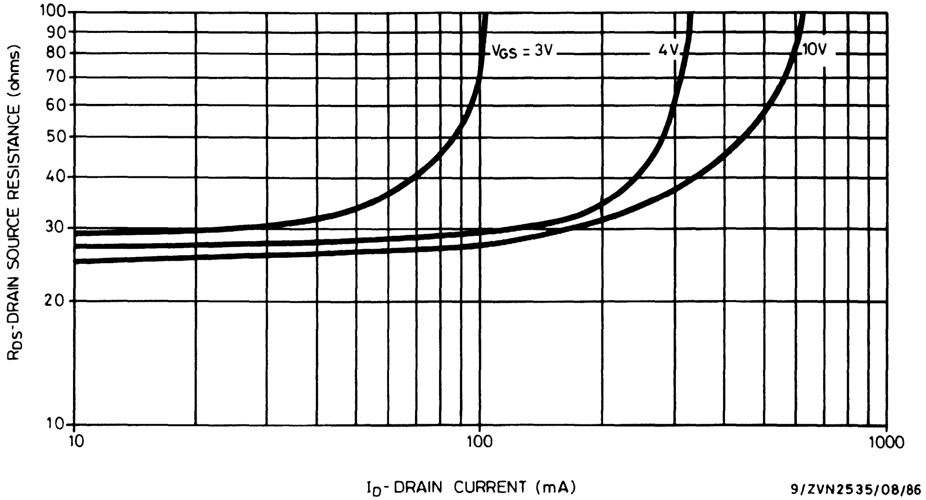


Fig. 9 Typical on-resistance v drain current

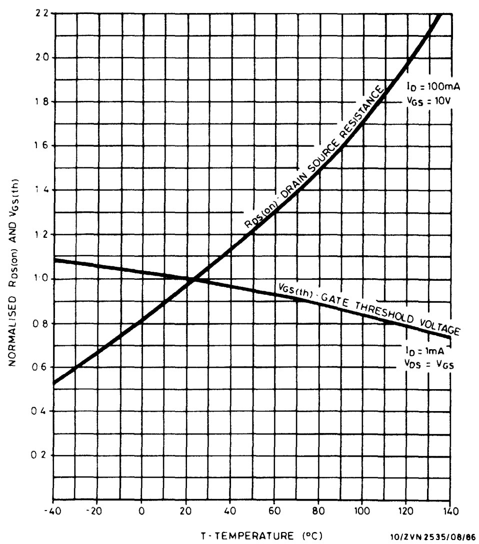


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

ZVN2535

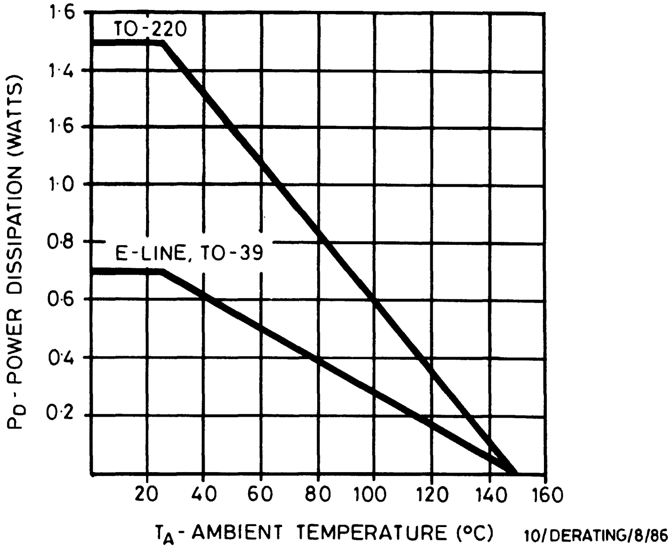


Fig. 11 Power v temperature derating curve (ambient)

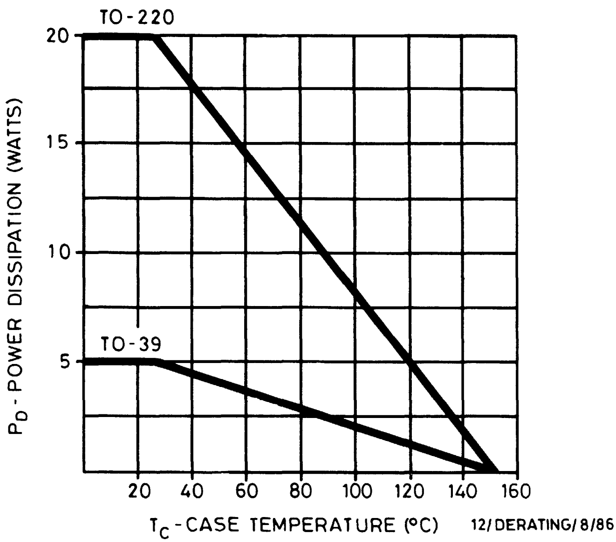


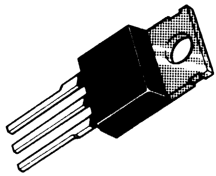
Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

ZVN3206

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-220
SUFFIX L

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN3206L*	60V	18A	0.12Ω

*BS-CECC approved

ZVN3206

ABSOLUTE MAXIMUM RATINGS

Parameter		TO-220	Unit
V_{DS}	Drain-source voltage	60	V
I_D	Continuous drain current (@ $T_C = 25°C$)	18	A
I_{DM}	Pulsed drain current	72	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_C = 25°C$)	75	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	V	$I_D = 250\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	2	4	V	$I_D = 250\mu A$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	500	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	250	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	1	mA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	18	–	A	$V_{DS} = 4V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	0.12	Ω	$I_D = 10A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	4	–	S	$V_{DS} = 10V$, $I_D = 10A$
C_{iss}	Input capacitance (2)	–	1500	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	750	pF	
C_{rss}	Reverse transfer capacitance (2)	–	250	pF	
$t_{d(on)}$	Turn-on delay time (2)	–	30	ns	$V_{DD} \approx 25V$, $I_D = 10A$ $Z_O = 15\Omega$
t_r	Rise time (2)	–	100	ns	
$t_{d(off)}$	Turn-off delay time (2)	–	50	ns	
t_f	Fall time (2)	–	60	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	1.08	V	$V_{GS}=0V$, $I_S=18A$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.

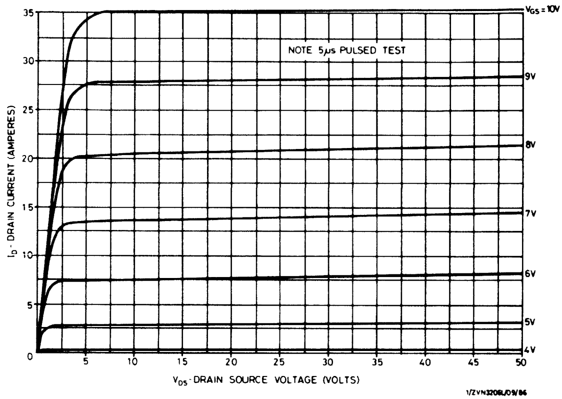


Fig. 1 Typical output characteristics

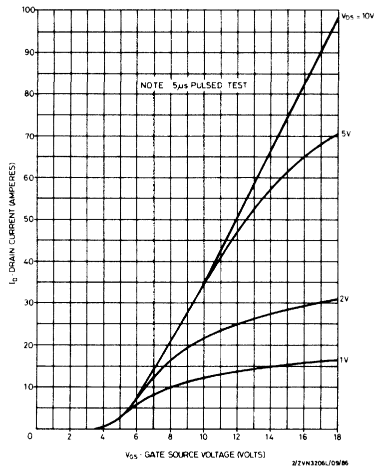


Fig. 2 Typical transfer characteristics

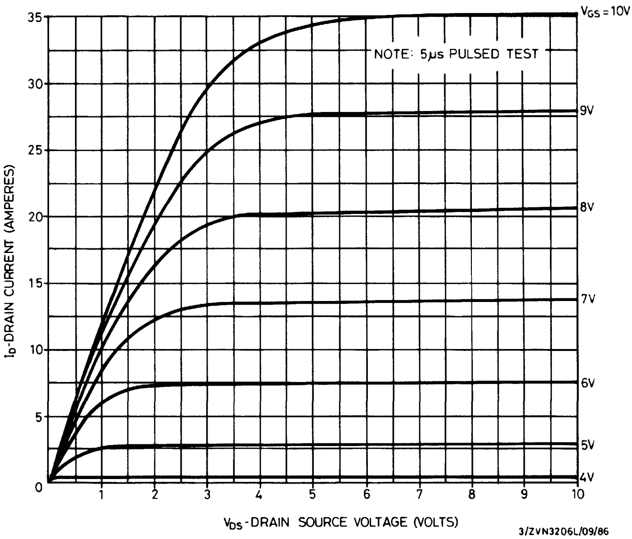


Fig. 3 Typical saturation characteristics

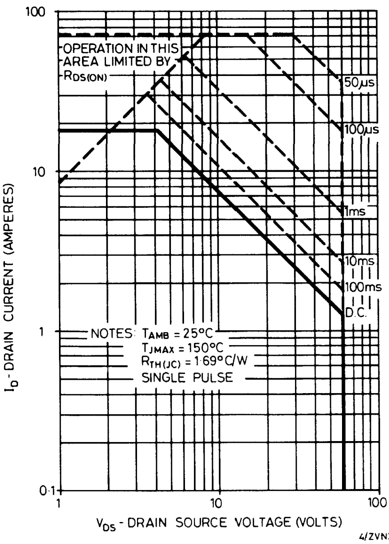


Fig. 4 Maximum safe operating area

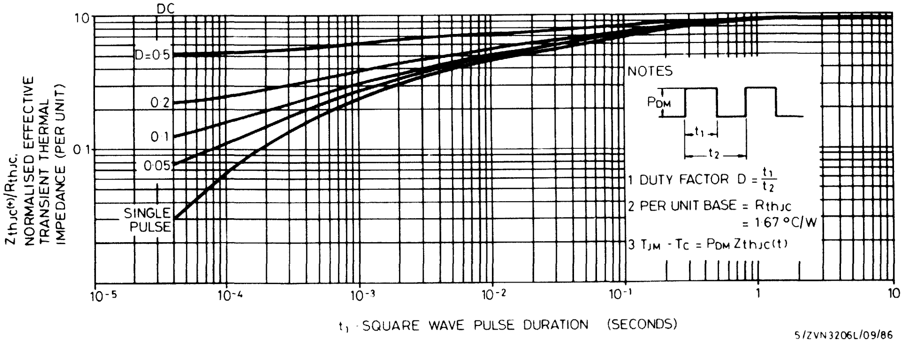


Fig. 5 Maximum effective transient thermal impedance, junction-to-case v pulse duration

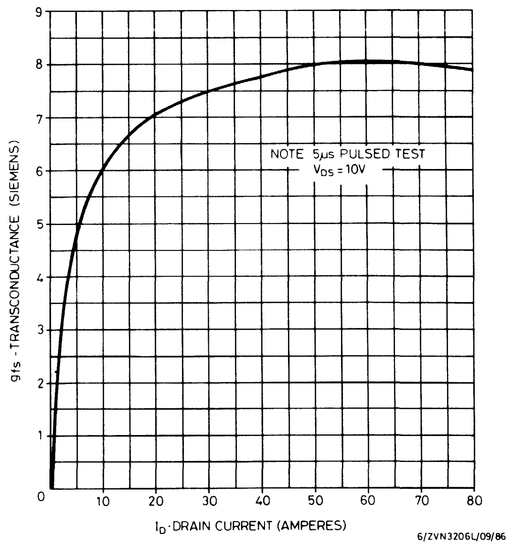


Fig. 6 Typical transconductance v drain current

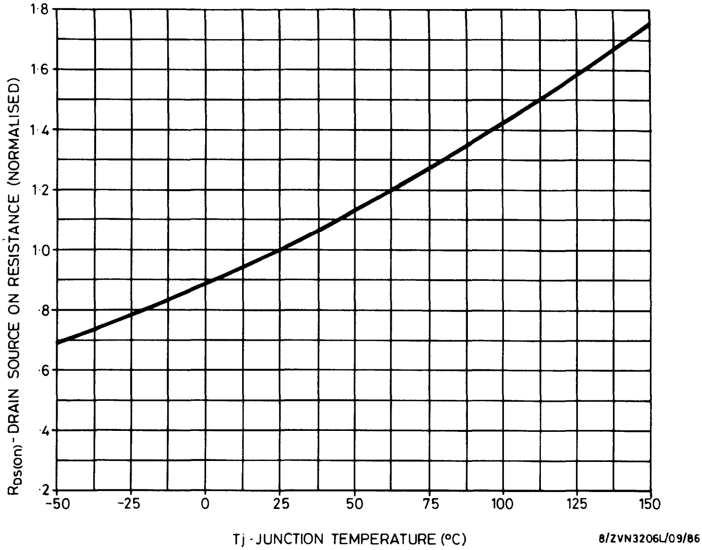


Fig. 7 Normalised on-resistance v temperature

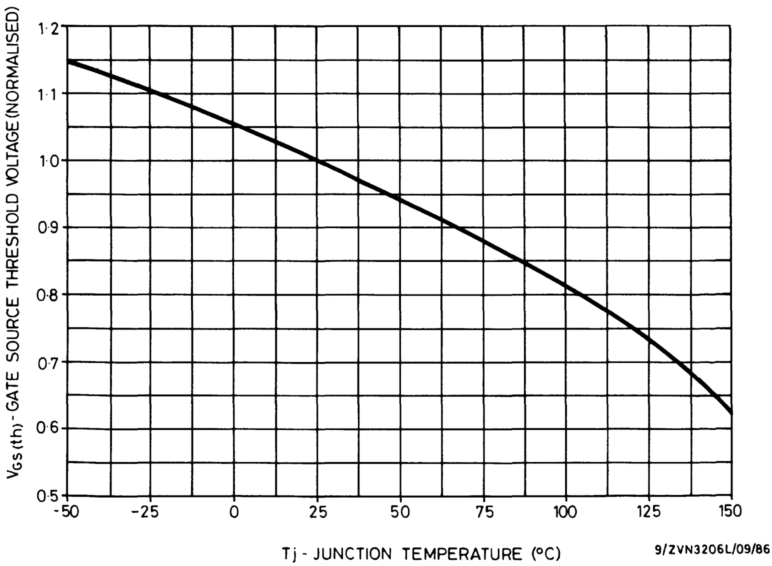


Fig. 8 Normalised gate threshold voltage v temperature

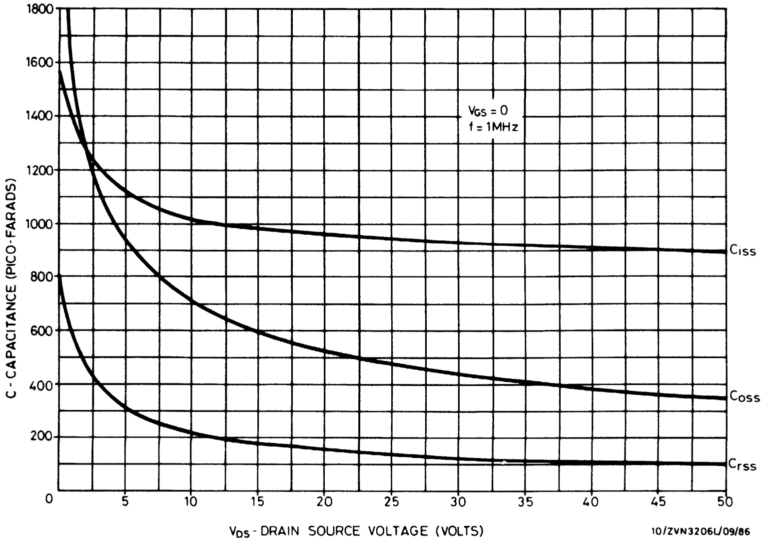


Fig. 9 Typical capacitance v drain-to-source voltage

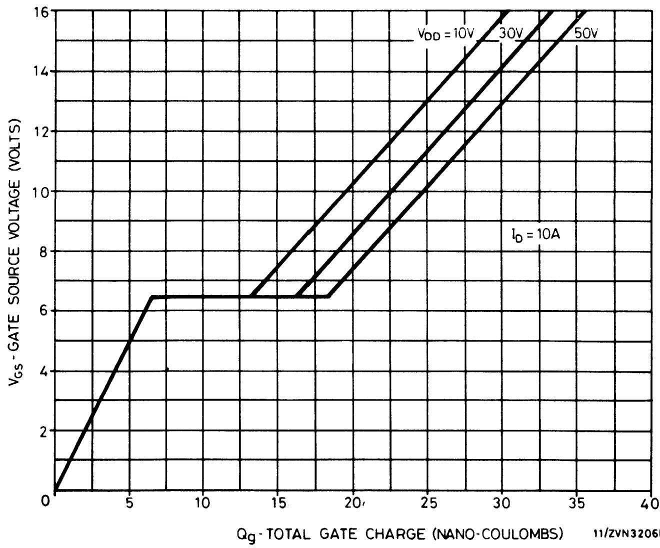


Fig. 10 Typical gate charge v gate-to-source voltage

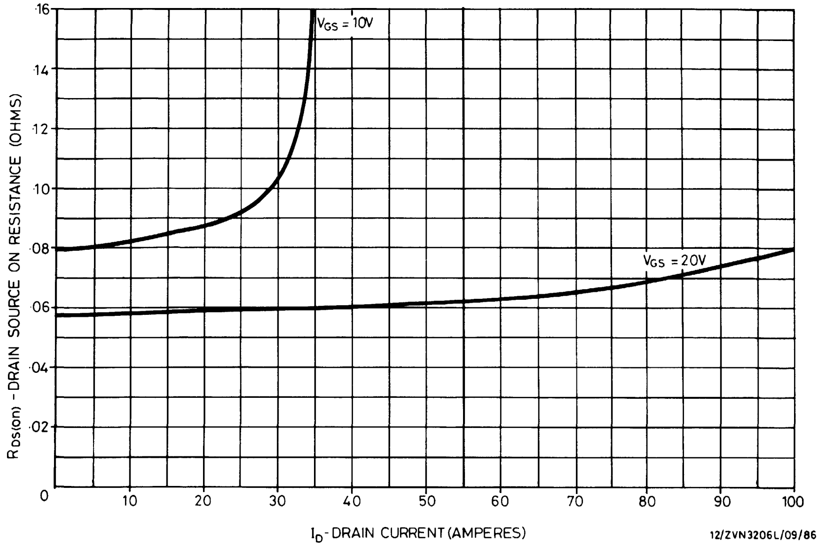


Fig. 11 Typical on-resistance v drain current

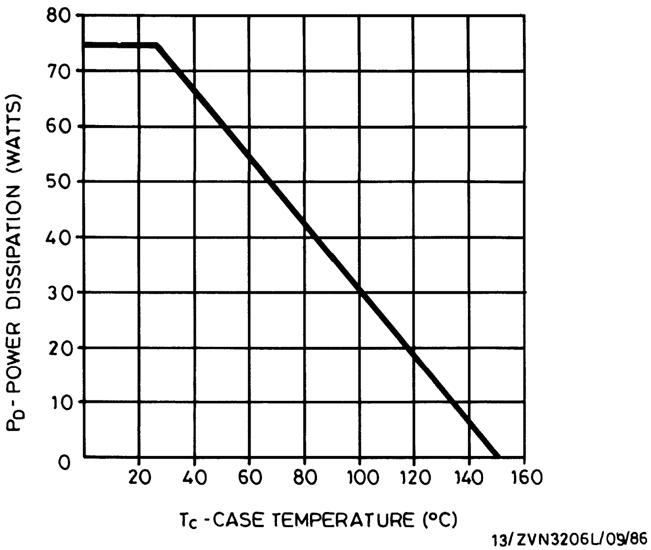


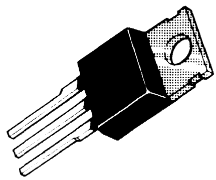
Fig. 12 Power v temperature derating curve

N-channel enhancement mode vertical DMOS FET

ZVN3210

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-220
SUFFIX L

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN3210L*	100V	14A	0.18Ω

*BS-CECC approved

ZVN3210

ABSOLUTE MAXIMUM RATINGS

	Parameter	TO-220	Unit
V_{DS}	Drain-source voltage	100	V
I_D	Continuous drain current (@ $T_C = 25°C$)	14	A
I_{DM}	Pulsed drain current	56	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_C = 25°C$)	75	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	100	–	V	$I_D = 250\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	2	4	V	$I_D = 250\mu A$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	500	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	250	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	1	mA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	14	–	A	$V_{DS} = 5V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	0.18	Ω	$I_D = 8A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	3	–	S	$V_{DS} = 10V$, $I_D = 8A$
C_{iss}	Input capacitance (2)	–	1200	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	500	pF	
C_{rss}	Reverse transfer capacitance (2)	–	150	pF	
$t_{d(on)}$	Turn-on delay time (2)	–	30	ns	$V_{DD} \approx 36V$, $I_D = 8A$ $Z_O = 15\Omega$
t_r	Rise time (2)	–	75	ns	
$t_{d(off)}$	Turn-off delay time (2)	–	40	ns	
t_f	Fall time (2)	–	45	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	1.0	V	$V_{GS} = 0V$, $I_S = 14A$

(1) Measured under pulsed conditions. Width = 300µs. Duty cycle ≤2%.
(2) Sample test.

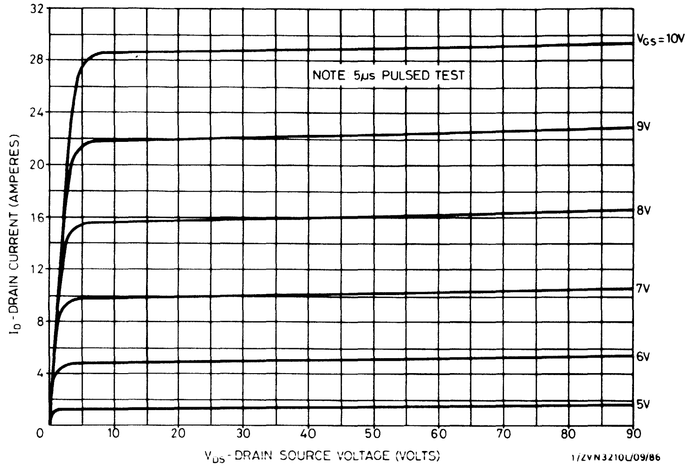


Fig. 1 Typical output characteristics

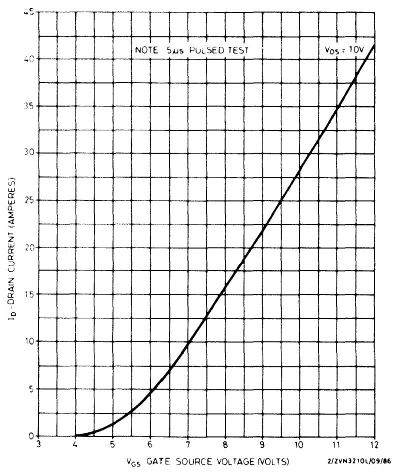


Fig. 2 Typical transfer characteristics

ZVN3210

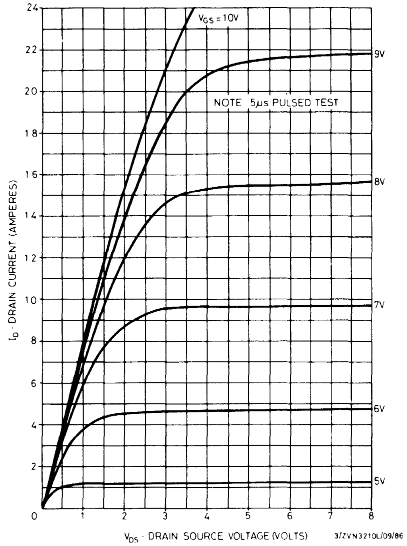


Fig. 3 Typical saturation characteristics

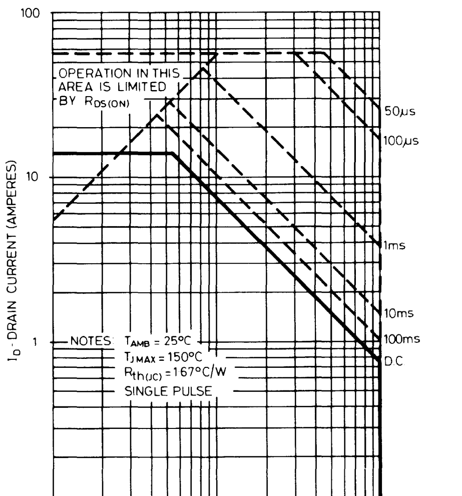


Fig. 4 Maximum safe operating area

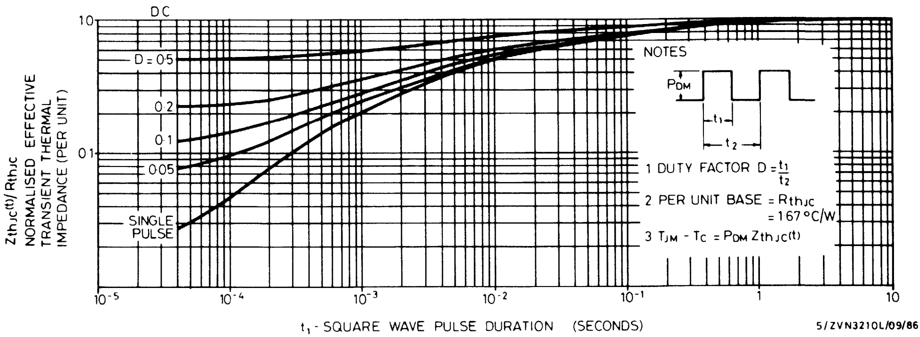


Fig. 5 Maximum effective transient thermal impedance, junction-to-case v pulse duration

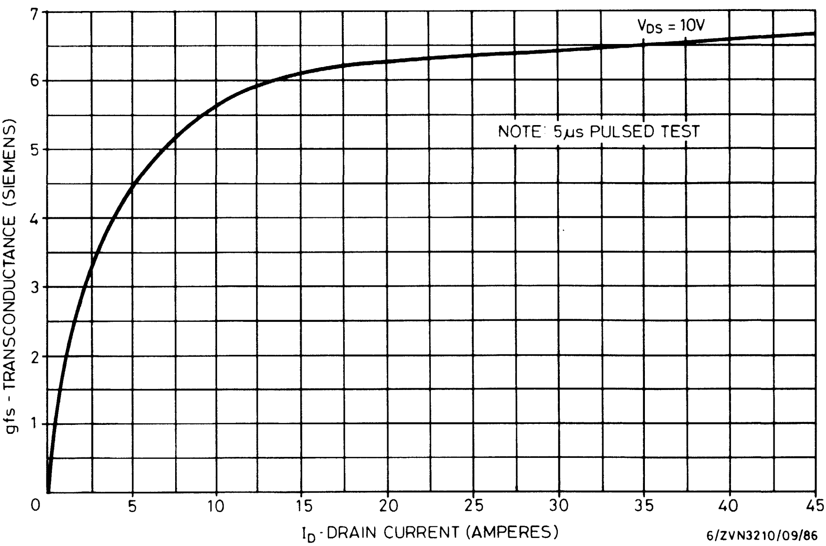


Fig. 6 Typical transconductance v drain current

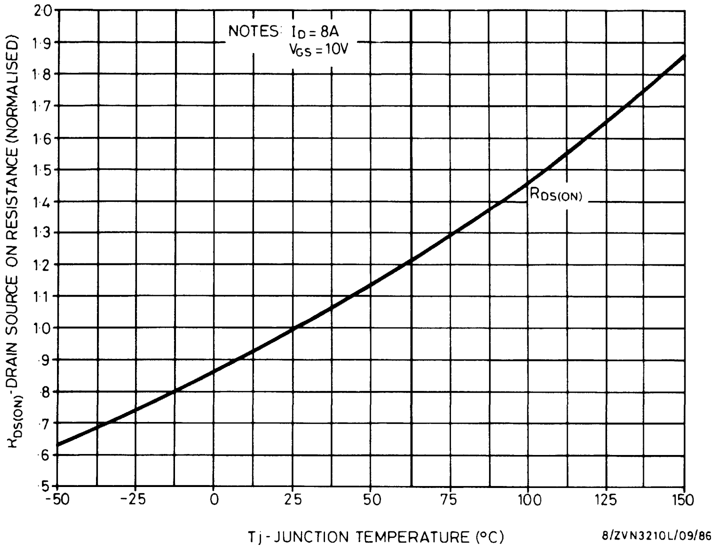


Fig. 7 Normalised on-resistance v temperature

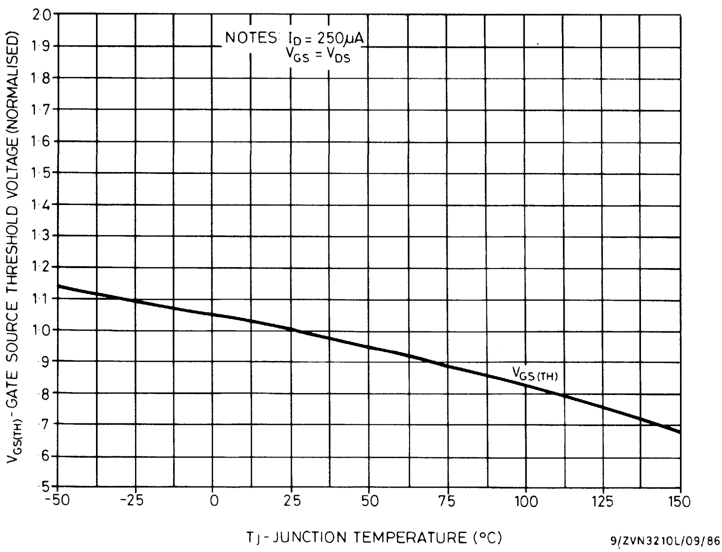


Fig. 8 Normalised gate threshold voltage v temperature

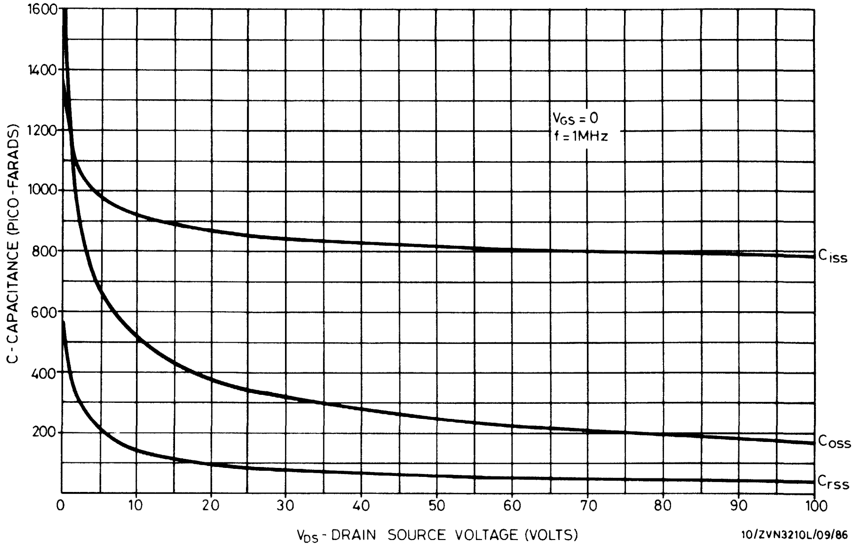


Fig. 9 Typical capacitance v drain-to-source voltage

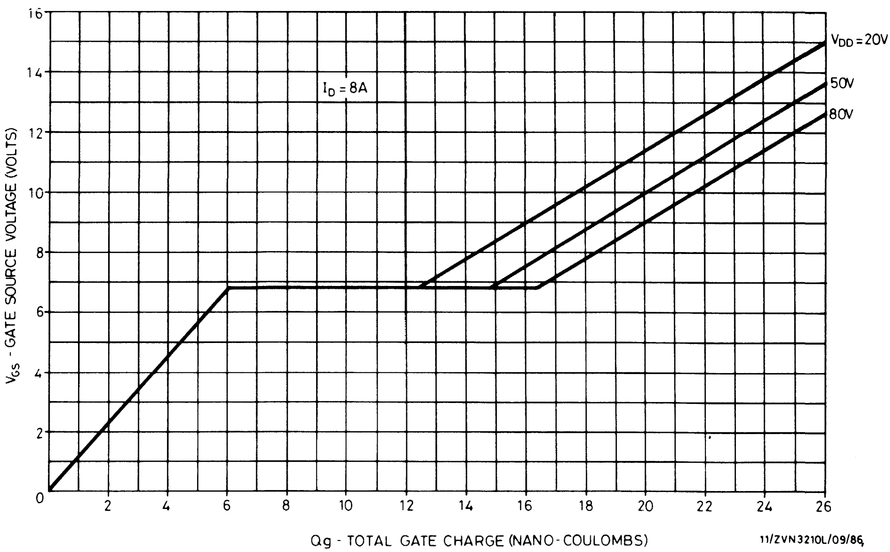


Fig. 10 Typical gate charge v gate-to-source voltage

ZVN3210

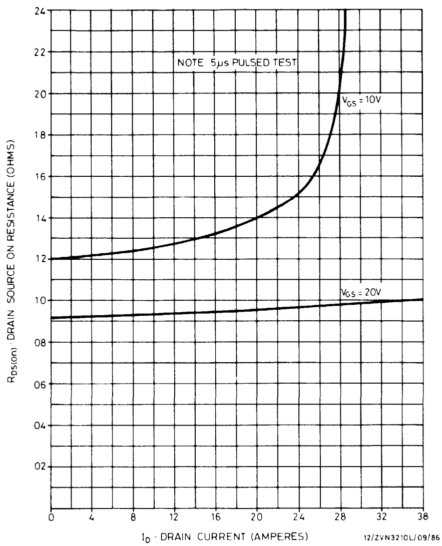


Fig. 11 Typical on-resistance v drain current

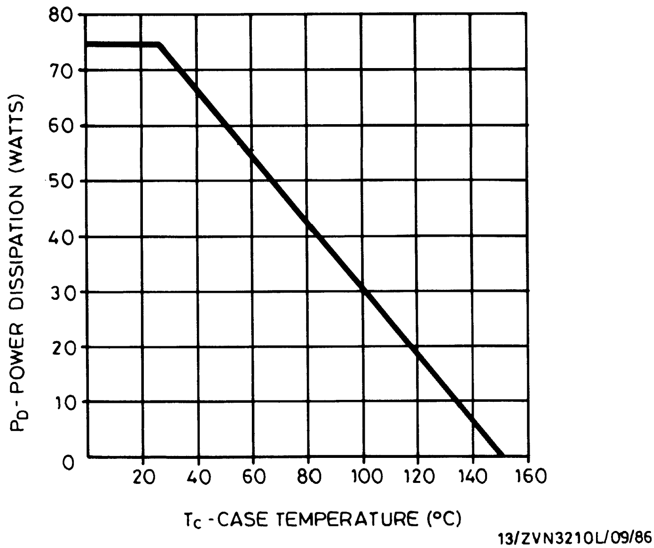


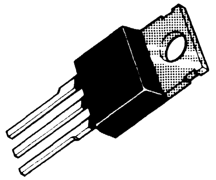
Fig. 12 Power v temperature derating curve

N-channel enhancement mode vertical DMOS FET

ZVN3220

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-220
SUFFIX L

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN3220L	200V	8A	0.5Ω

ZVN3220

ABSOLUTE MAXIMUM RATINGS

	Parameter	TO-220	Unit
V_{DS}	Drain-source voltage	200	V
I_D	Continuous drain current (@ $T_C = 25°C$)	8	A
I_{DM}	Pulsed drain current	32	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_C = 25°C$)	75	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	–	V	$I_D = 250\mu A$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	2	4	V	$I_D = 250\mu A$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	500	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	250	µA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	1	mA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	8	–	A	$V_{DS} = 10V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	0.5	Ω	$I_D = 5A$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	2.5	–	S	$V_{DS} = 10V$, $I_D = 5A$
C_{iss}	Input capacitance (2)	–	1200	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	450	pF	
C_{rss}	Reverse transfer capacitance (2)	–	150	pF	
$t_{d(on)}$	Turn-on delay time (2)	–	30	ns	$V_{DD} \approx 90V$, $I_D = 5A$ $Z_O = 15\Omega$
t_r	Rise time (2)	–	50	ns	
$t_{d(off)}$	Turn-off delay time (2)	–	50	ns	
t_f	Fall time (2)	–	40	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.94	V	$V_{GS}=0V$, $I_S=8A$

(1) Measured under pulsed conditions. Width = 300µs. Duty cycle ≤ 2%.
(2) Sample test.

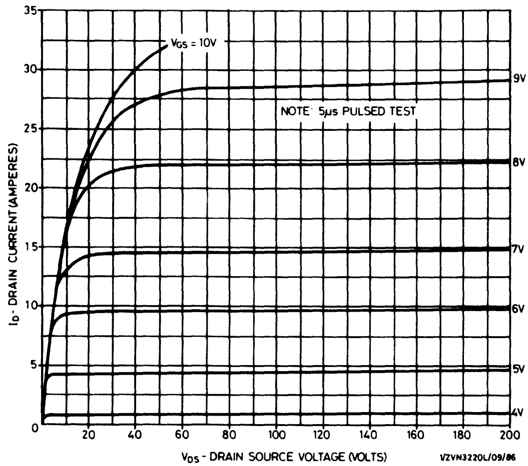


Fig. 1 Typical output characteristics

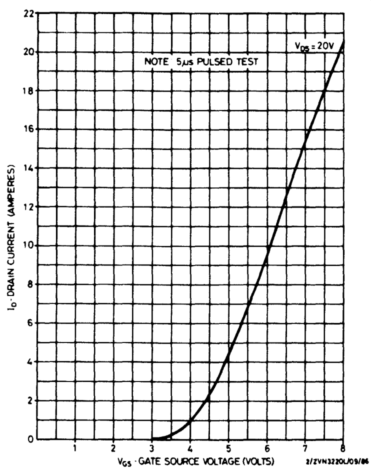


Fig. 2 Typical transfer characteristics

ZVN3220

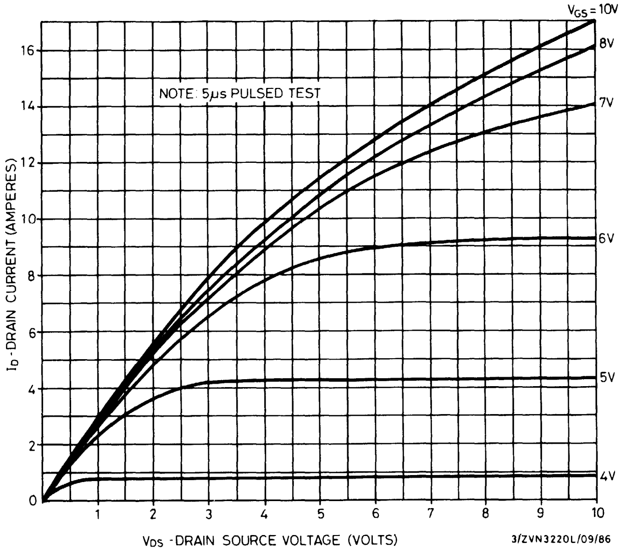


Fig. 3 Typical saturation characteristics

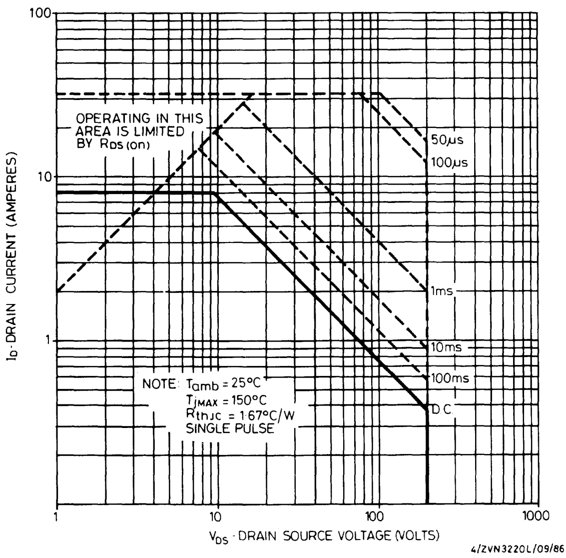


Fig. 4 Maximum safe operating area

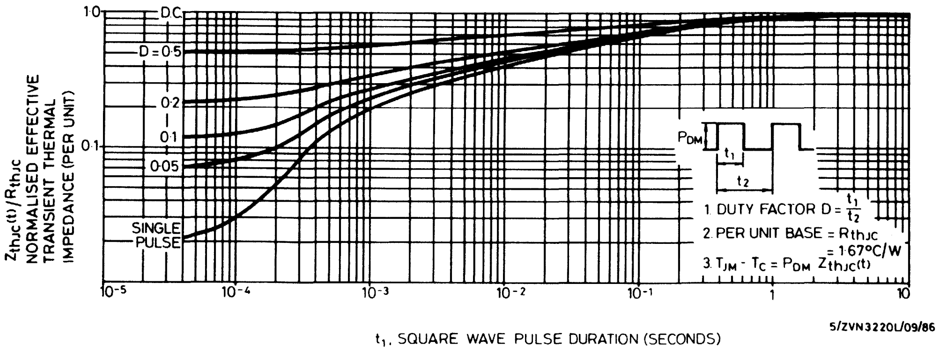


Fig. 5 Maximum effective transient thermal impedance, junction-to-case v pulse duration

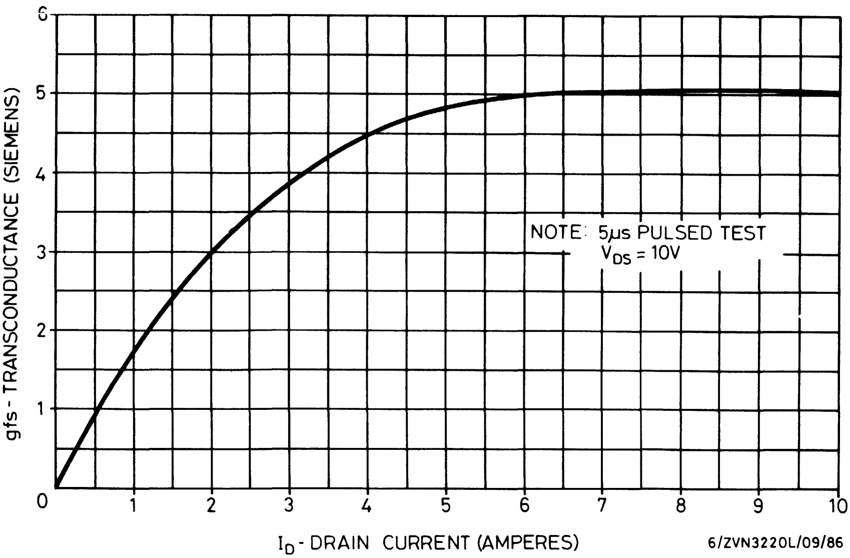


Fig. 6 Typical transconductance v drain current

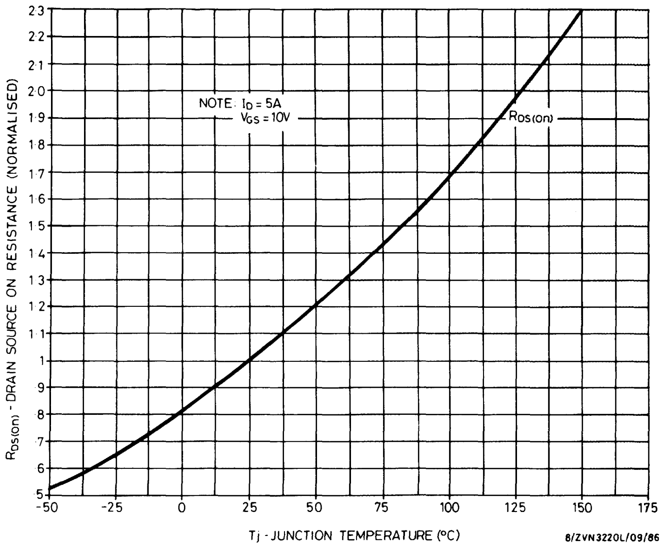


Fig. 7 Normalised on-resistance v temperature

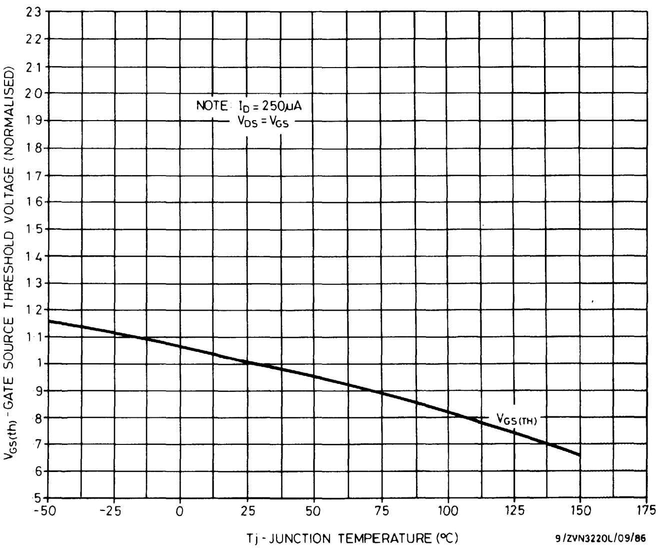


Fig. 8 Normalised gate threshold voltage v temperature

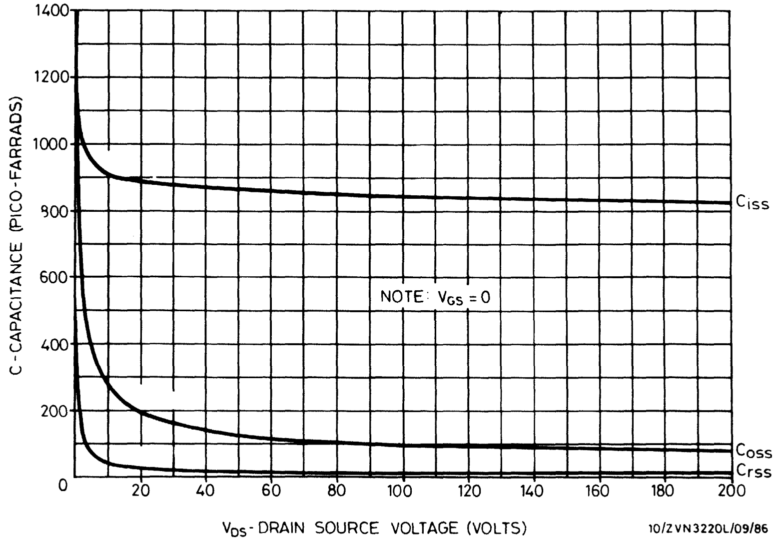


Fig. 9 Typical capacitance v drain-to-source voltage

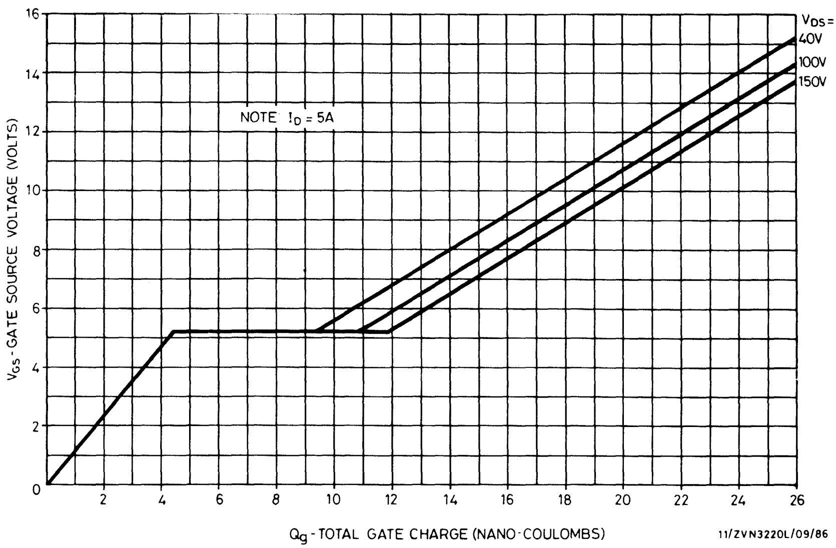


Fig. 10 Typical gate charge v gate-to-source voltage

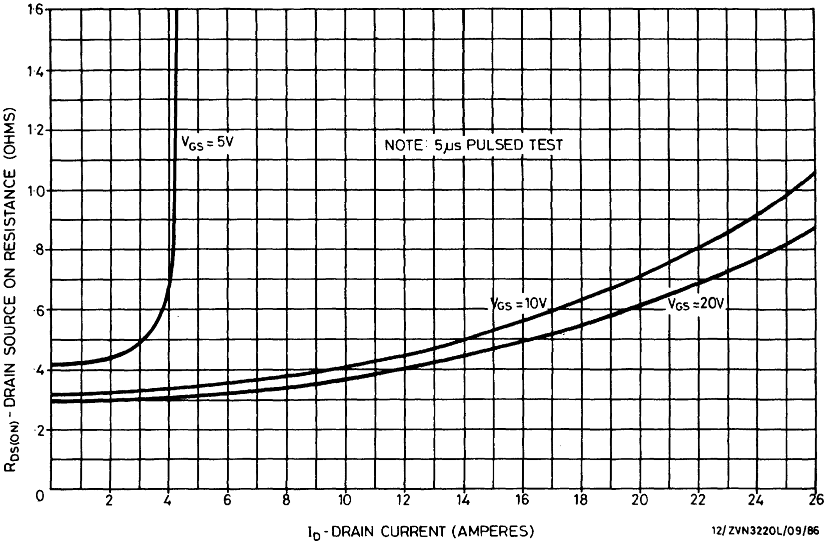


Fig. 11 Typical on-resistance v drain current

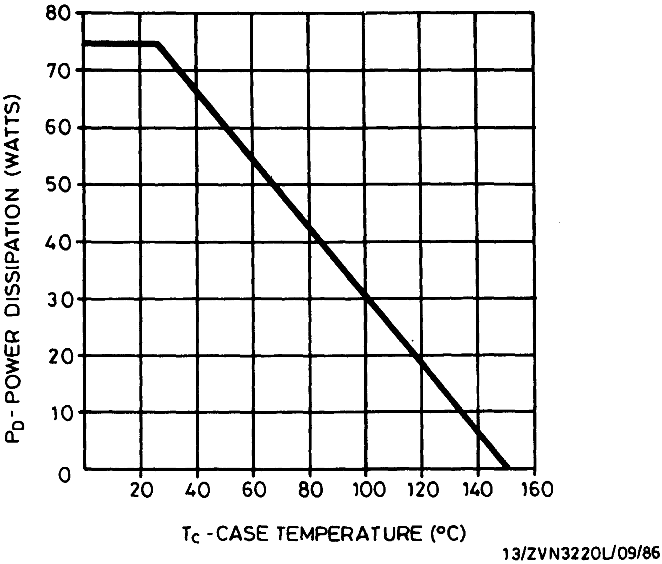


Fig. 12 Power v temperature derating curve

N-channel enhancement mode vertical DMOS FET

ZVN3306

FEATURES

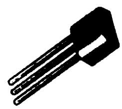
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

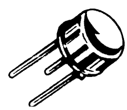
A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

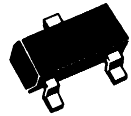
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN3306A	60V	0.27A	5Ω
ZVN3306B	60V	0.75A	5Ω
ZVN3306F	60V	0.15A	5Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



SOT-23
SUFFIX F

ZVN3306

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	SOT-23	Units
V_{DS}	Drain-source voltage	60	60	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.27	0.27	0.15	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.75	–	A
I_{DM}	Pulse drain current	3	3	3	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.625	0.25	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	0.5	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	750	–	–	mA	$V_{DS} = 18V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	5	Ω	$I_D = 500mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	150	–	–	mS	$V_{DS} = 18V$, $I_D = 500mA$
C_{iss}	Input capacitance (2)	–	–	35	pF	$V_{DS} = 18V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	8	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3	5	ns	$V_{DD} \approx 18V$, $I_D = 500mA$
t_r	Rise time (2) (3)	–	4	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	4	6	ns	
t_f	Fall time (2) (3)	–	5	8	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.85	V	$V_{GS}=0V$, $I_S=270mA$
t_{rr}	Reverse recovery time	90	ns	$V_{GS}=0V$, $I_F=270mA$ $I_R=100mA$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle $\leqslant$2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

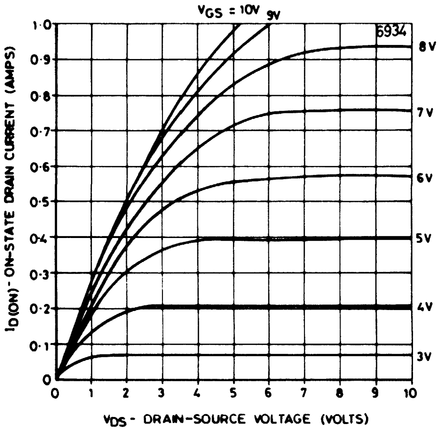


Fig. 1 Typical saturation characteristics

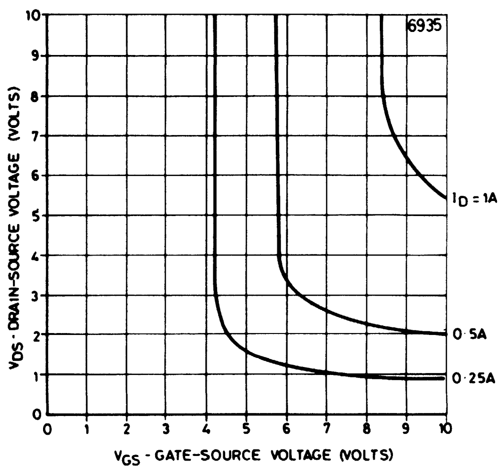


Fig. 2 Typical voltage saturation characteristics

ZVN3306

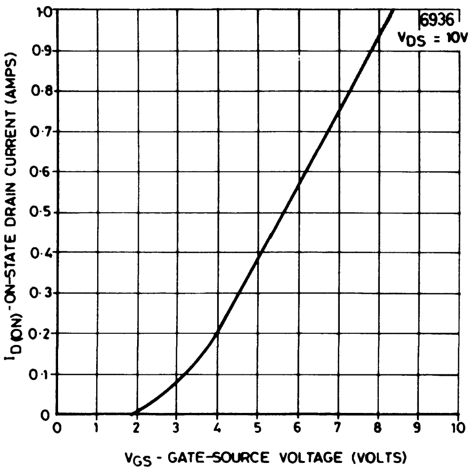


Fig. 3 Typical transfer characteristics

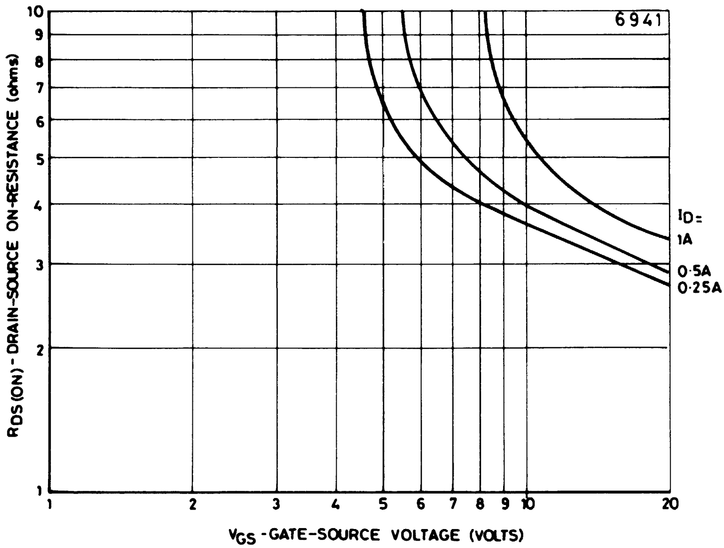


Fig. 4 Typical on-resistance v gate-source voltage

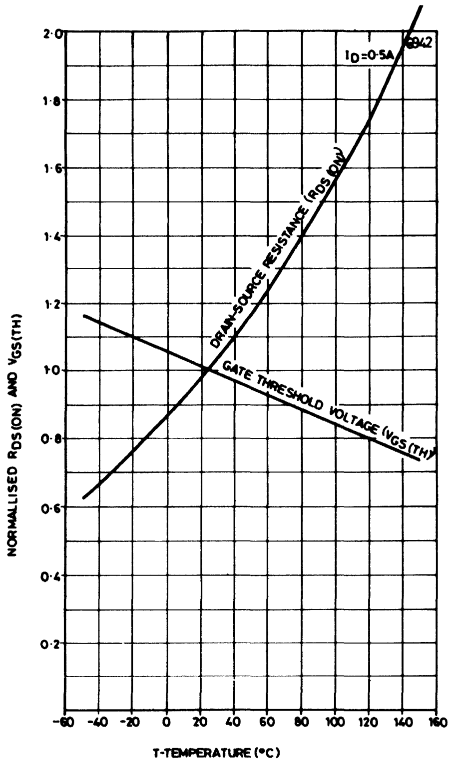


Fig. 5 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

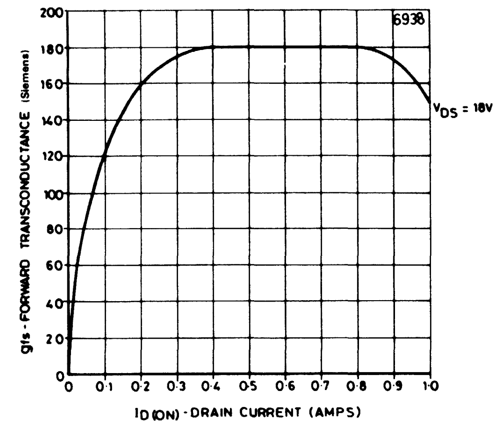


Fig. 6 Typical transconductance v drain current

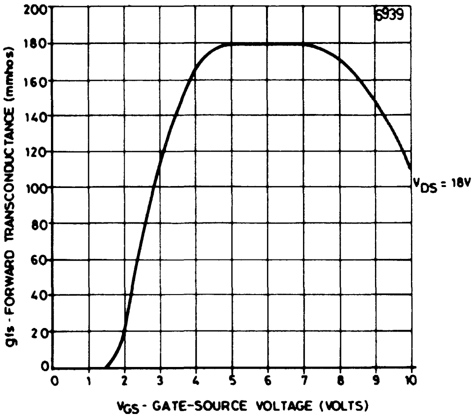


Fig. 7 Typical transconductance v gate-source voltage

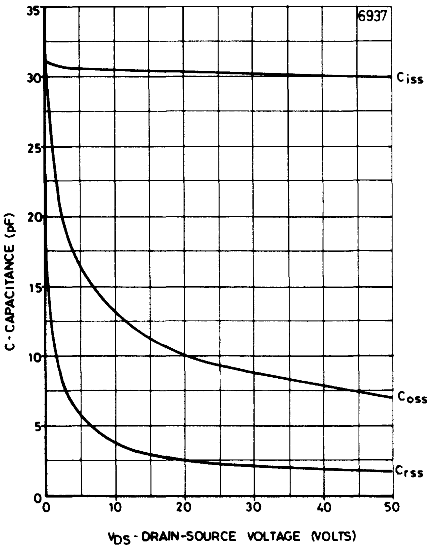


Fig. 8 Typical capacitance v drain-source voltage

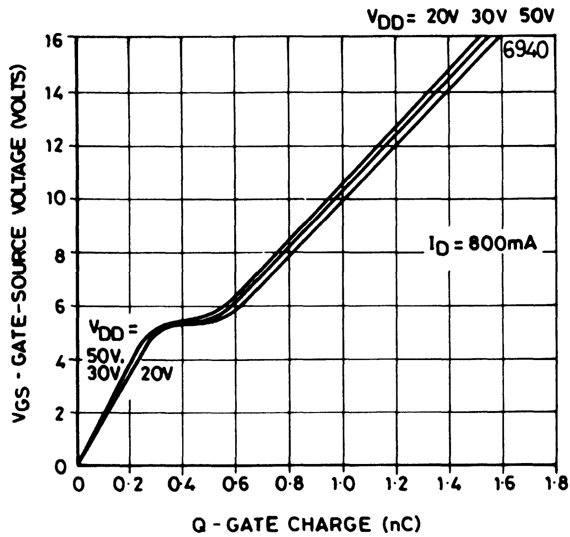


Fig. 9 Typical gate charge v gate-source voltage

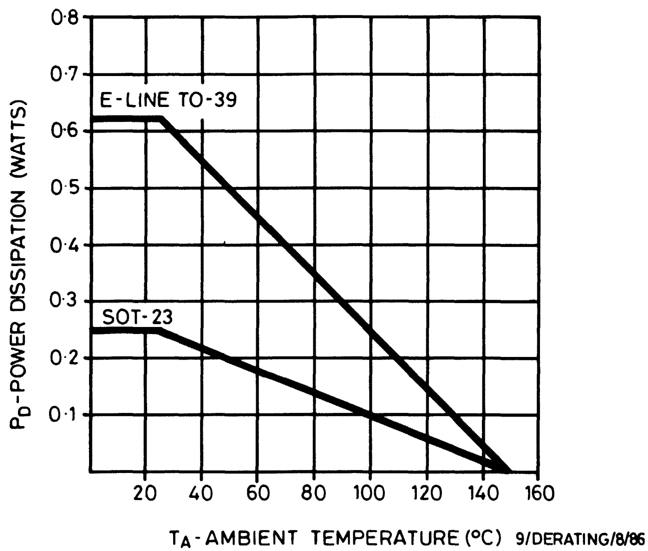


Fig. 10 Power v temperature derating curve (ambient)

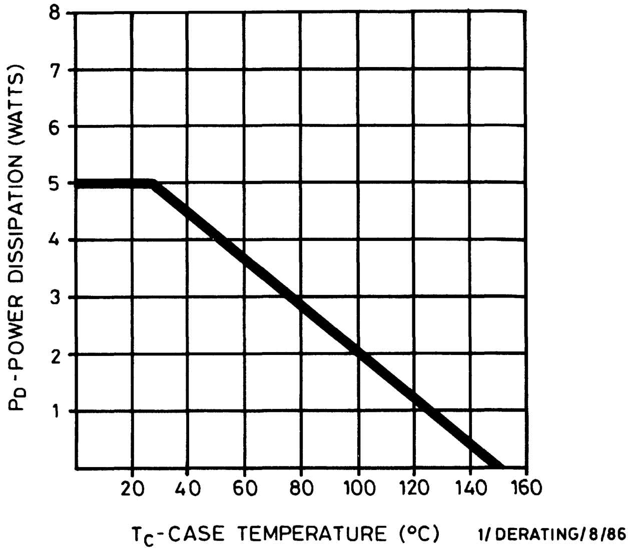


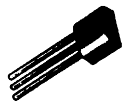
Fig. 11 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

ZVN3310

FEATURES

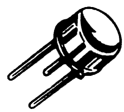
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

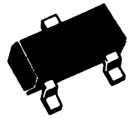
A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.



TO-39
SUFFIX B

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN3310A	100V	0.2A	10Ω
ZVN3310B	100V	0.5A	10Ω
ZVN3310F	100V	0.1A	10Ω



SOT-23
SUFFIX F

ZVN3310

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	SOT-23	Units
V_{DS}	Drain-source voltage	100	100	100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.2	0.2	0.1	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.5	–	A
I_{DM}	Pulse drain current	2	2	2	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.625	0.25	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	100	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	0.8	–	2.4	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	1	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	500	–	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	10	Ω	$I_D = 500mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	100	–	–	mS	$V_{DS} = 25V$, $I_D = 500mA$
C_{iss}	Input capacitance (2)	–	–	40	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	–	15	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	3	5	ns	$V_{DD} \approx 25V$, $I_D = 500mA$
t_r	Rise time (2) (3)	–	5	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	4	6	ns	
t_f	Fall time (2) (3)	–	5	7	ns	

SOURCE-DRAIN DIODE CHARACTERISTICS

	Parameter	Typ.	Unit	Conditions
V_{SD}	Diode forward voltage (1)	0.82	V	$V_{GS}=0V$, $I_S=200mA$

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

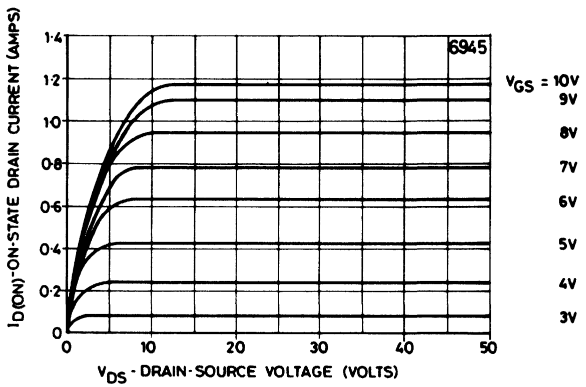


Fig. 1 Typical output characteristics

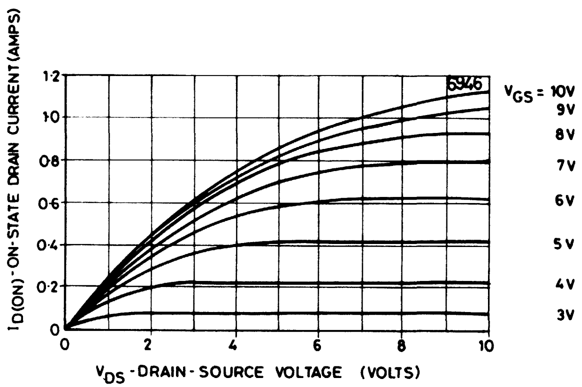


Fig. 2 Typical saturation characteristics

ZVN3310

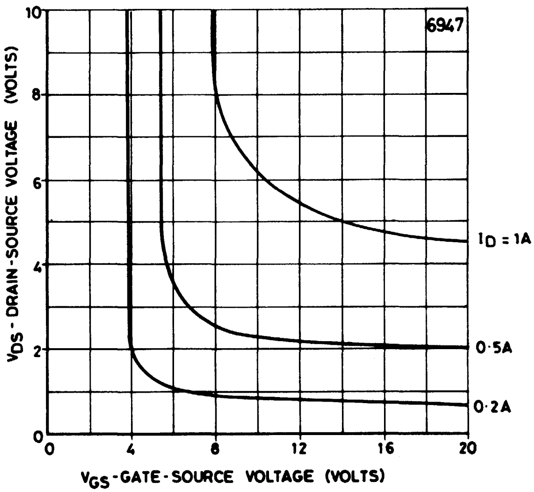


Fig. 3 Typical voltage saturation characteristics

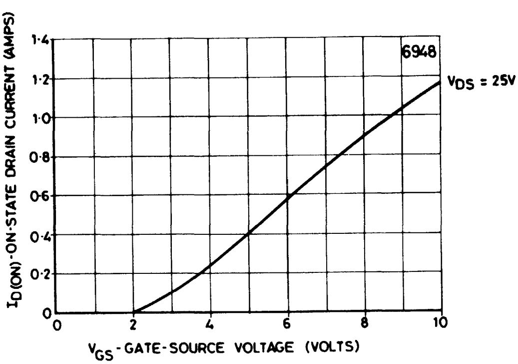


Fig. 4 Typical transfer characteristics

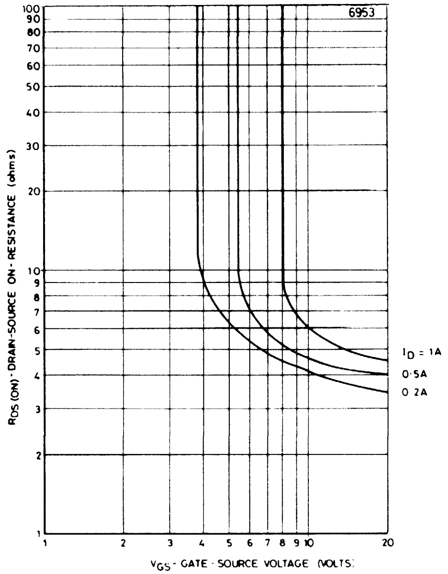


Fig. 5 Typical on-resistance v gate-source voltage

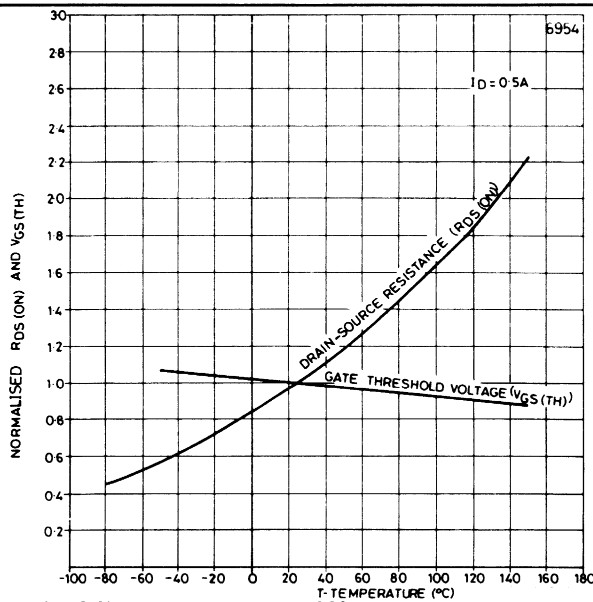


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

ZVN3310

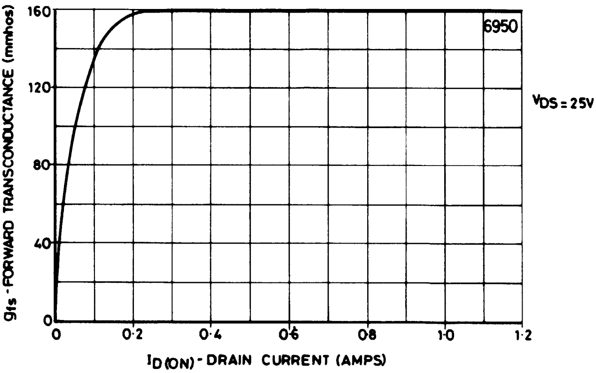


Fig. 7 Typical transconductance v drain current

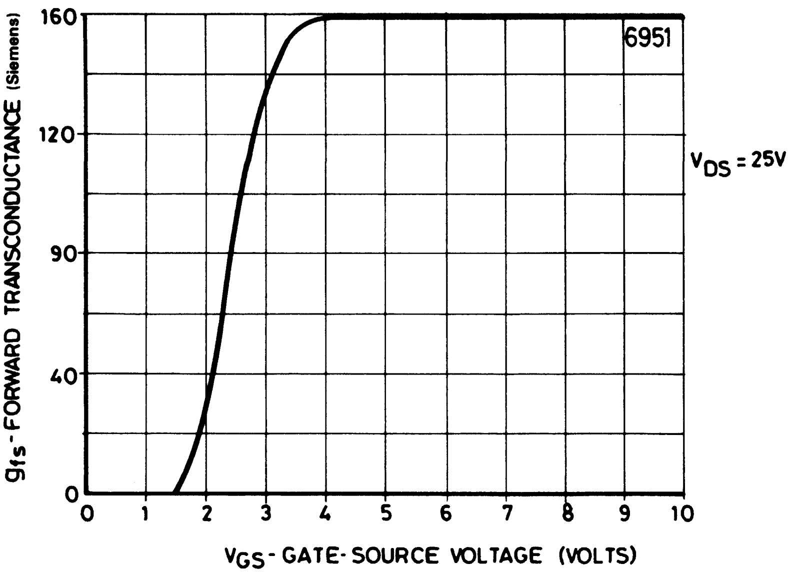


Fig. 8 Typical transconductance v gate-source voltage

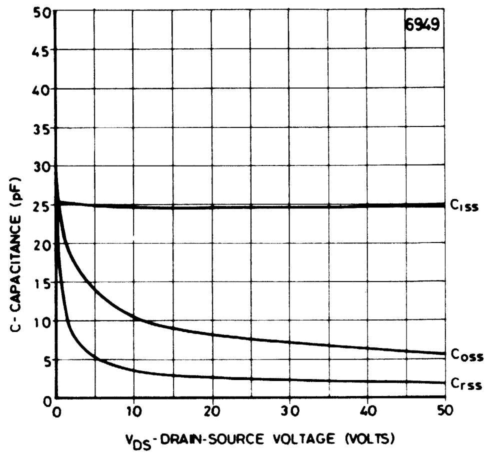


Fig. 9 Typical capacitance v drain-source voltage

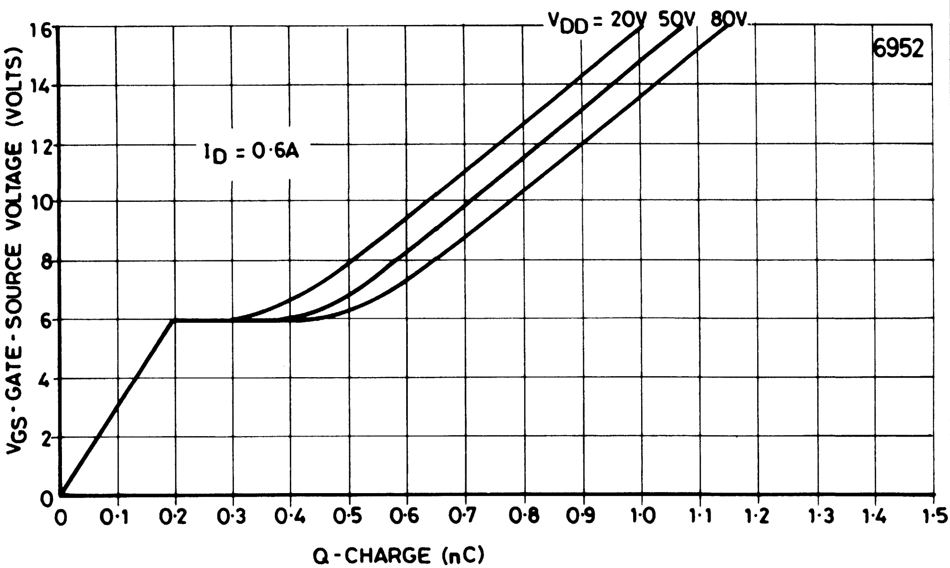


Fig. 10 Typical gate charge v gate-source voltage

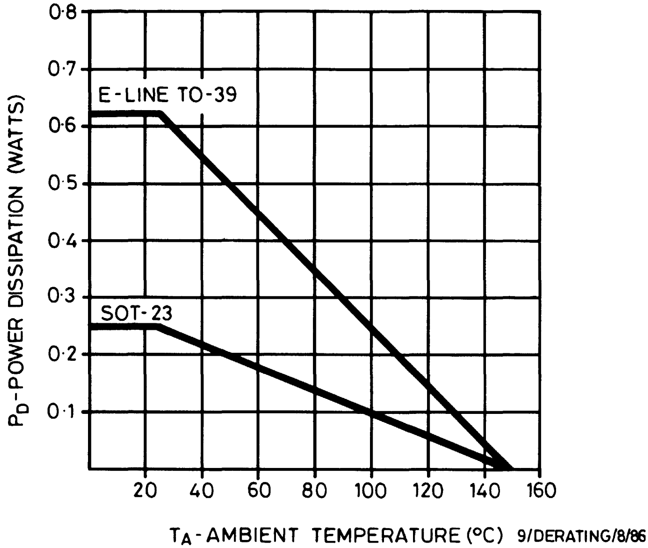


Fig. 11 Power v temperature derating curve (ambient)

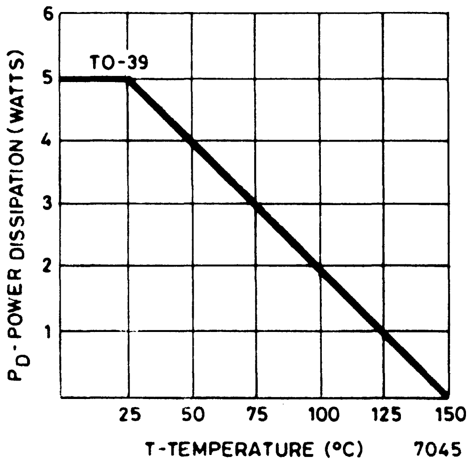


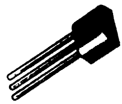
Fig. 12 Power v temperature derating curve (case)

N-channel enhancement mode vertical DMOS FET

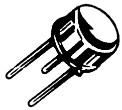
ZVN3320

FEATURES

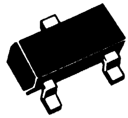
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



SOT-23
SUFFIX F

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN3320A	200V	0.1A	25Ω
ZVN3320B	200V	0.25A	25Ω
ZVN3320F	200V	0.06A	25Ω

ZVN3320

ABSOLUTE MAXIMUM RATINGS

	Parameter	E-line	TO-39	SOT-23	Units
V_{DS}	Drain-source voltage	200	200	200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.1	0.1	0.06	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	0.25	–	A
I_{DM}	Pulse drain current	1	1	1	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.625	0.25	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	–55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	200	–	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1	–	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	0.1	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	250	–	–	mA	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	25	Ω	$I_D = 100mA$, $V_{GS} = 10V$
g_{fs}	Forward transconductance (1) (2)	75	–	–	mS	$V_{DS} = 25V$, $I_D = 100mA$
C_{iss}	Input capacitance (2)	–	–	45	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	–	18	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	–	5	ns	$V_{DD} \approx 25V$, $I_D = 100mA$
t_r	Rise time (2) (3)	–	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	–	6	ns	
t_f	Fall time (2) (3)	–	–	6	ns	

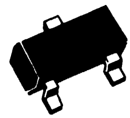
(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement mode vertical DMOS FET

ZVN4106

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



SOT-23
SUFFIX F

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN4106F	60V	0.2A	2.5Ω

ZVN4106

ABSOLUTE MAXIMUM RATINGS

Parameters		SOT-23	Unit
V_{DS}	Drain-source voltage	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.2	A
I_{DM}	Pulse drain current	3	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.25	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1.3	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	1	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	2.5	Ω	$I_D = 500mA$, $V_{GS} = 10V$
		–	5	Ω	$I_D = 200mA$, $V_{GS} = 5V$
g_{fs}	Forward transconductance (1) (2)	150	–	mS	$V_{DS} = 25V$, $I_D = 500mA$
C_{iss}	Input capacitance (2)	–	35	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	8	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	5	ns	$V_{DD} \approx 25V$, $I_D = 500mA$
t_r	Rise time (2) (3)	–	7	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	6	ns	
t_f	Fall time (2) (3)	–	8	ns	

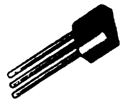
(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

N-channel enhancement mode vertical DMOS FET

ZVN4206

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A

DESCRIPTION

A compact cell geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVN4206A	60V	0.6A	1Ω

ZVN4206

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	Unit
V_{DS}	Drain-source voltage	60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	0.6	A
I_{DM}	Pulse drain current	8	A
V_{GS}	Gate-source voltage	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150	°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	60	–	V	$I_D = 1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	1.3	3	V	$I_D = 1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	3	–	A	$V_{DS} = 25V$, $V_{GS} = 10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	1	Ω	$I_D = 1.5A$, $V_{GS} = 10V$
		–	1.5	Ω	$I_D = 0.5A$, $V_{GS} = 5V$
g_{fs}	Forward transconductance (1) (2)	0.3	–	S	$V_{DS} = 25V$, $I_D = 1.5A$
C_{iss}	Input capacitance (2)	–	100	pF	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	60	pF	
C_{rss}	Reverse transfer capacitance (2)	–	20	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx 25V$, $I_D = 1.5A$
t_r	Rise time (2) (3)	–	12	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator.

P-channel enhancement mode vertical DMOS FET

ZVP0120

FEATURES

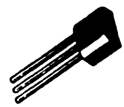
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

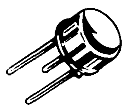
A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

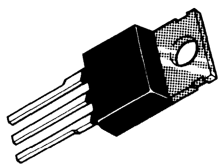
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP0120A	-200V	-0.11A	32Ω
ZVP0120B	-200V	-0.25A	32Ω
ZVP0120L	-200V	-0.25A	32Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVP0120

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	−200	−200	−200	V
I_D	Continuous drain current (@ $T_A=25°C$)	−0.11	−0.11	−0.14	A
I_D	Continuous drain current (@ $T_C=25°C$)	–	−0.25	−0.25	A
I_{DM}	Pulse drain current	−1	−1	−1	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A=25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C=25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−200	–	V	$I_D=-1mA$, $V_{GS}=0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D=-1mA$, $V_{DS}=V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS}=\pm20V$, $V_{DS}=0V$
I_{DSS}	Zero gate voltage drain current	–	−10	μA	V_{DS} = Max. rating, $V_{GS}=0V$
		–	−100	μA	$V_{DS}=0.8\times$ Max. rating $V_{GS}=0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−250	–	mA	$V_{DS}=-25V$, $V_{GS}=-10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	32	Ω	$I_D=-125mA$, $V_{GS}=-10V$
g_{fs}	Forward transconductance (1) (2)	50	–	mS	$V_{DS}=-25V$, $I_D=-125mA$
C_{iss}	Input capacitance (2)	–	100	pF	$V_{DS}=-25V$, $V_{GS}=0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD}\approx-25V$, $I_D=-125mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

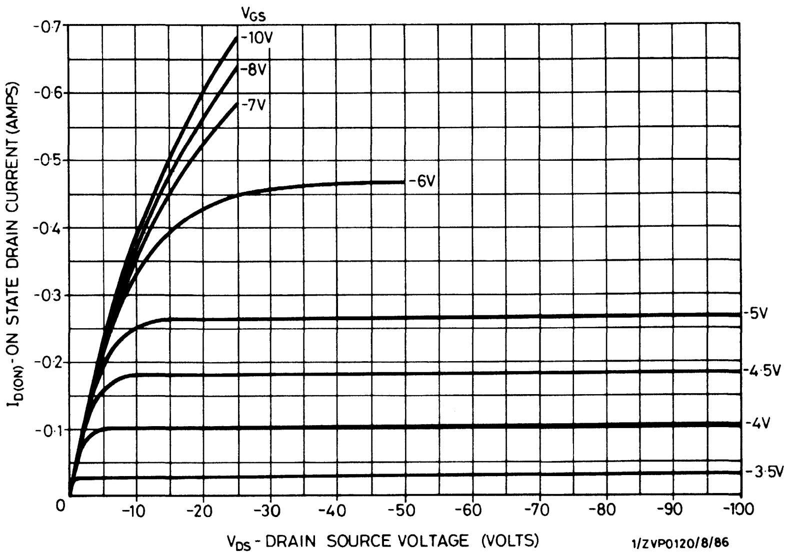


Fig. 1 Typical output characteristics

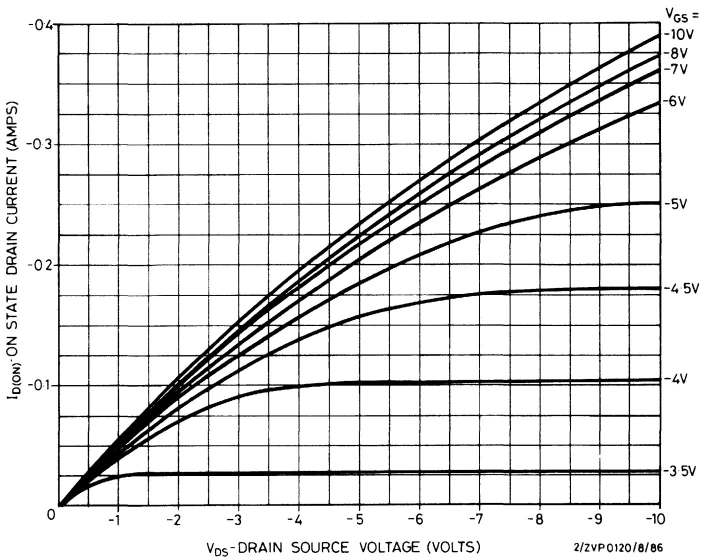


Fig. 2 Typical saturation characteristics

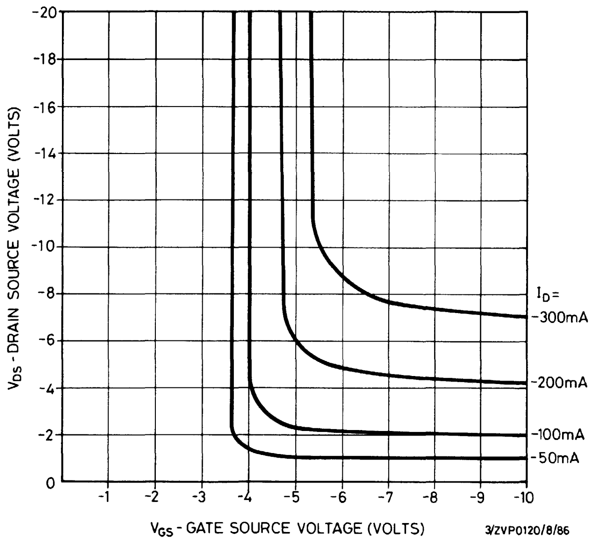


Fig. 3 Typical voltage saturation characteristics

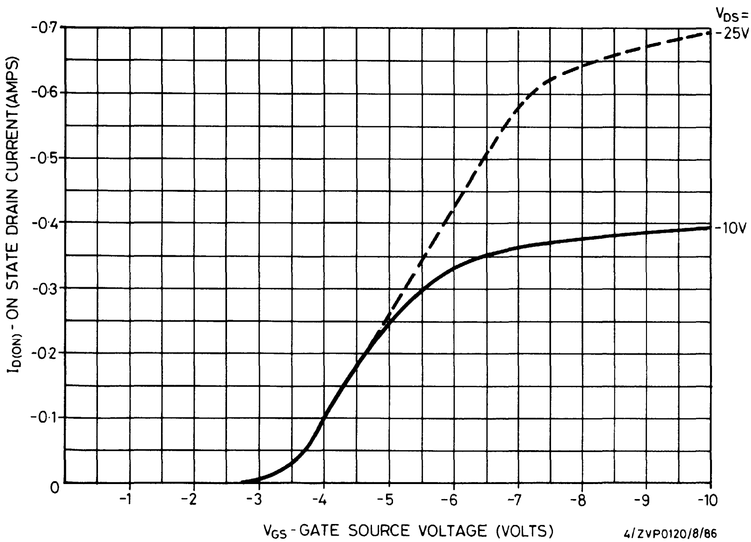


Fig. 4 Typical transfer characteristics

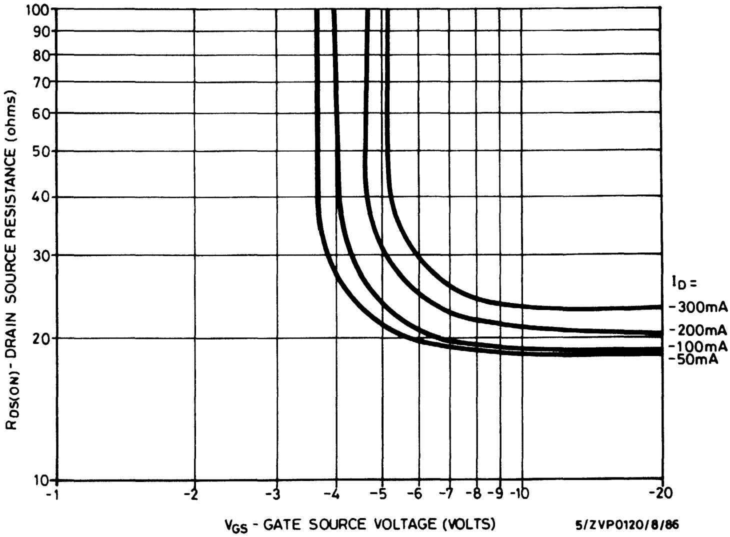


Fig. 5 Typical on-resistance v gate-source voltage

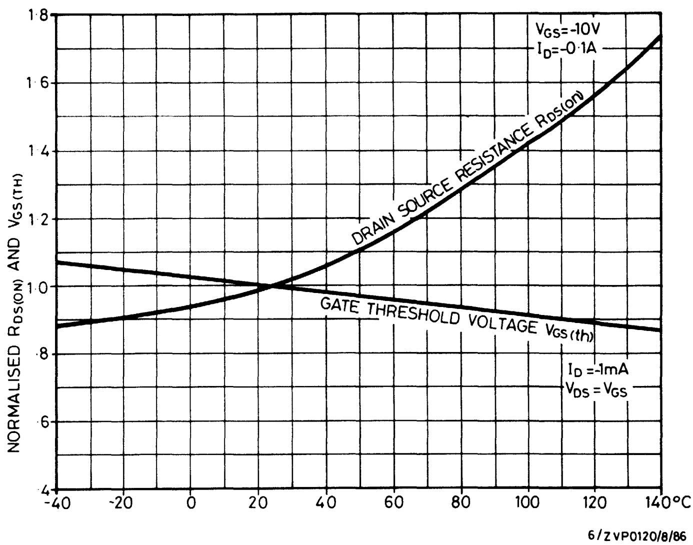


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

ZVP0120

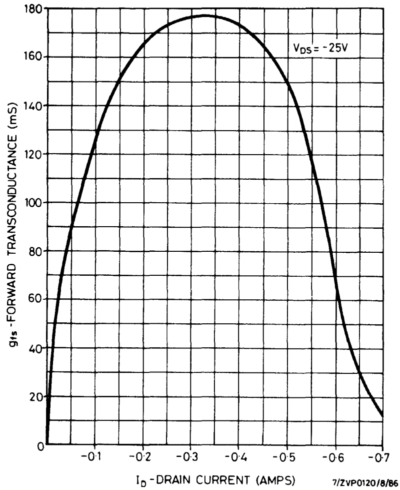


Fig. 7 Typical transconductance v drain current

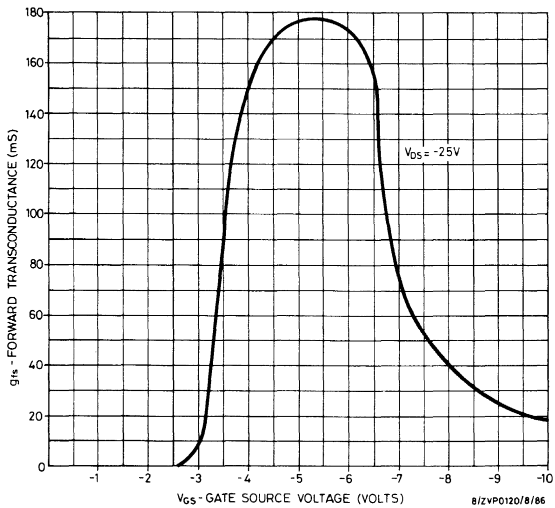


Fig. 8 Typical transconductance v gate-source voltage

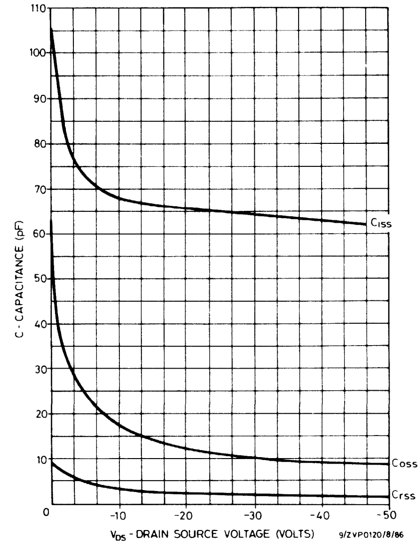


Fig. 9 Typical capacitance v drain-source voltage

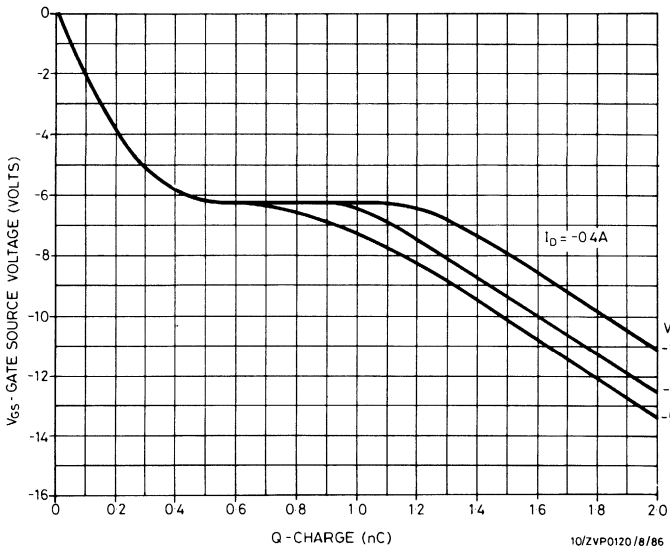


Fig. 10 Typical gate charge v gate-source voltage

ZVP0120

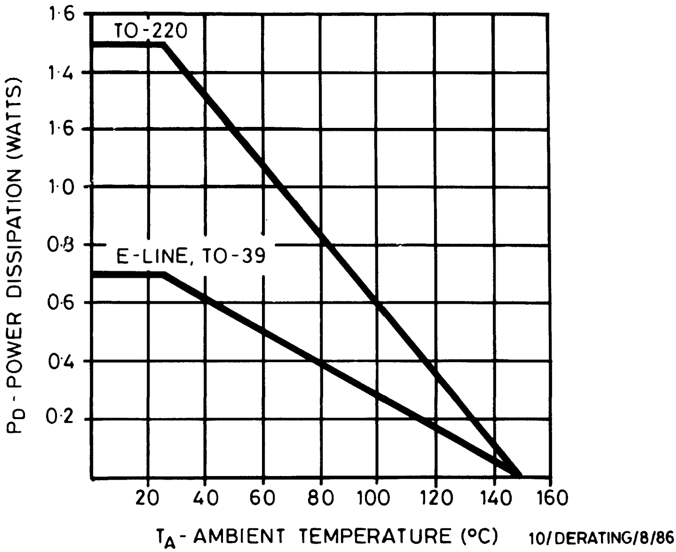


Fig. 11 Power v temperature derating curve (ambient)

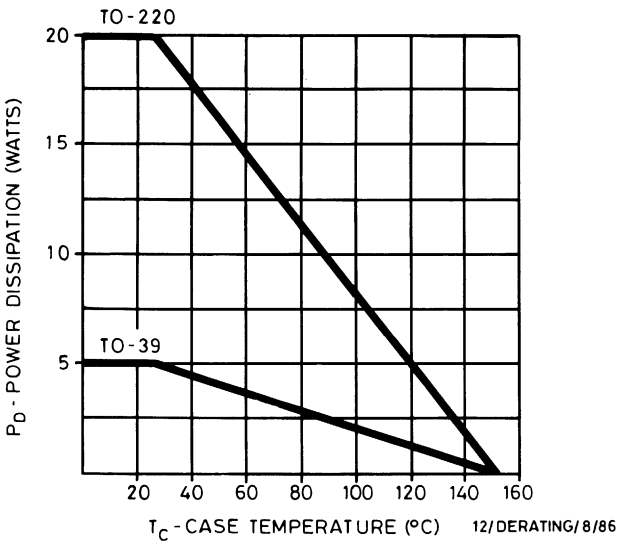


Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

ZVP0535

FEATURES

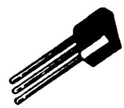
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

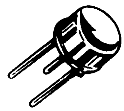
A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

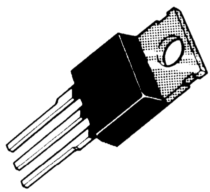
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP0535A	−350V	−0.05A	100Ω
ZVP0535B	−350V	−0.12A	100Ω
ZVP0535L	−350V	−0.12A	100Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVP0535

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	−350	−350	−350	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.05	−0.05	−0.08	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.12	−0.12	A
I_{DM}	Pulse drain current	−0.48	−0.48	−0.48	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−350	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−4.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−20	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−2	mA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−120	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	100	Ω	$I_D = -50mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	40	–	mS	$V_{DS} = -25V$, $I_D = -50mA$
C_{iss}	Input capacitance (2)	–	120	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	10	ns	$V_{DD} \approx -25V$, $I_D = -50mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	15	ns	
t_f	Fall time (2) (3)	–	20	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

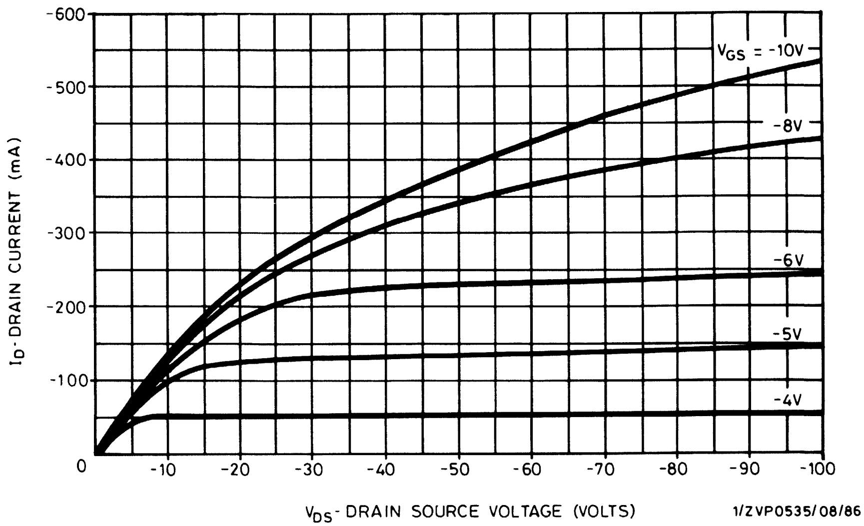


Fig. 1 Typical output characteristics

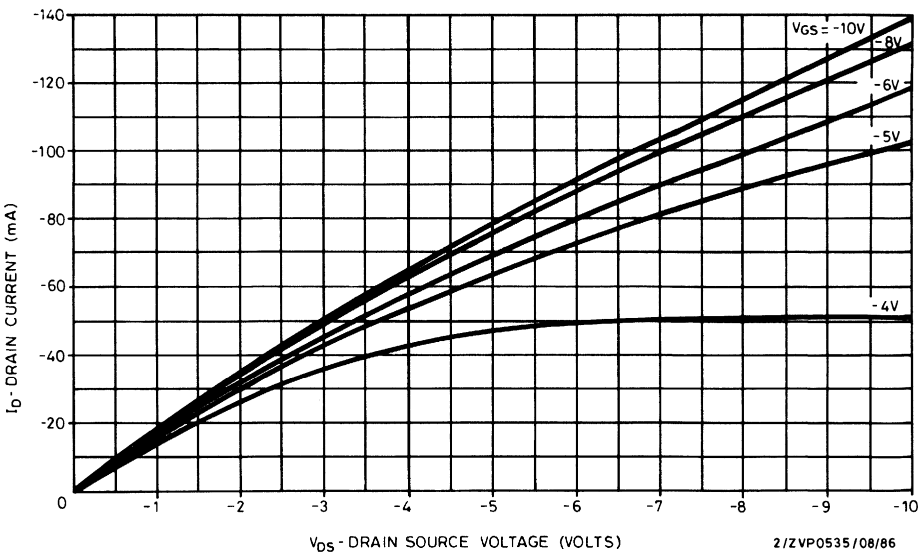


Fig. 2 Typical saturation characteristics

ZVP0535

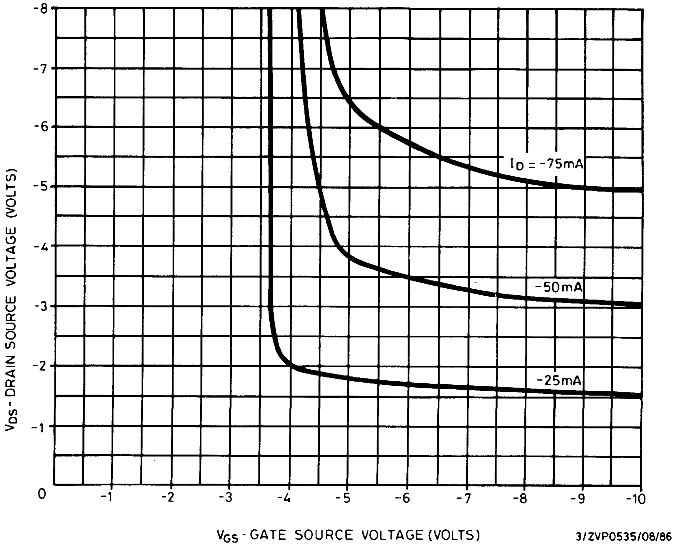


Fig. 3 Typical voltage saturation characteristics

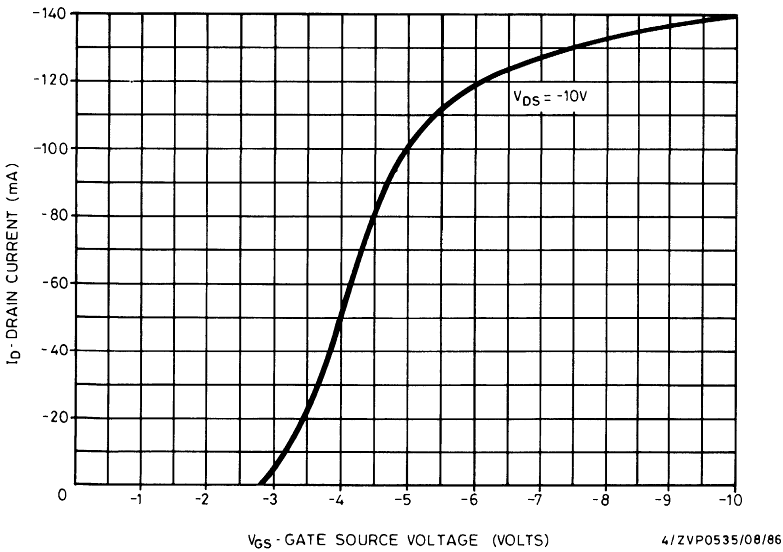


Fig. 4 Typical transfer characteristics

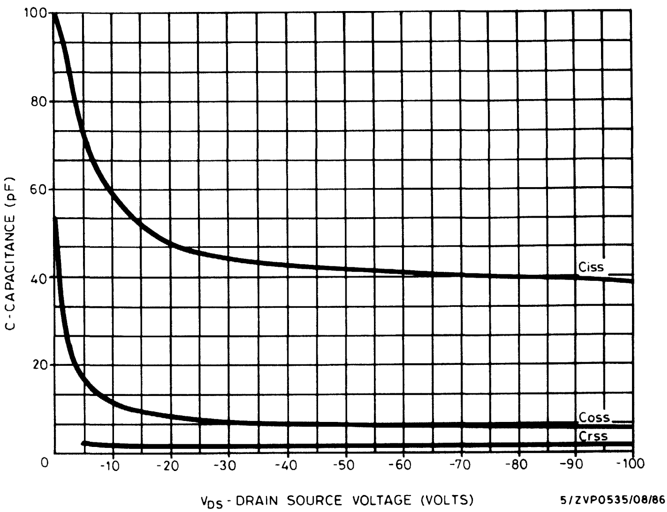


Fig. 5 Typical capacitance v drain-source voltage

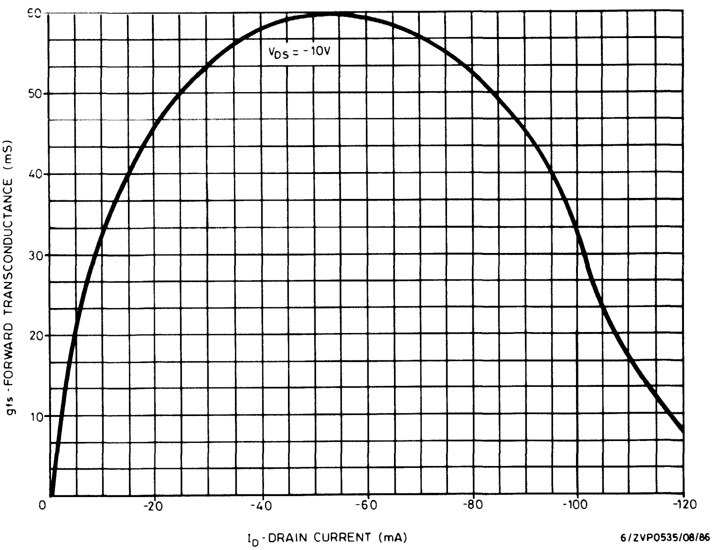


Fig. 6 Typical transconductance v drain current

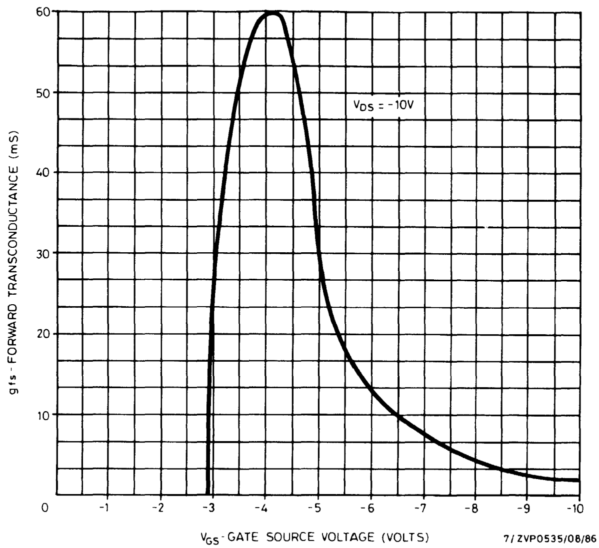


Fig. 7 Typical transconductance v gate-source voltage

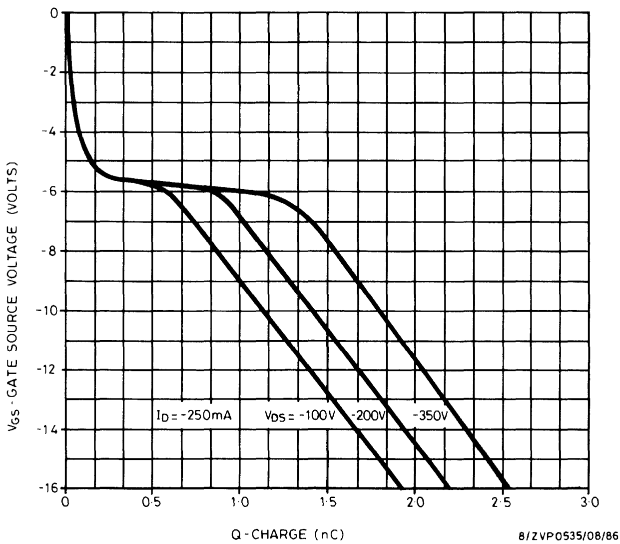


Fig. 8 Typical gate charge v gate-source voltage

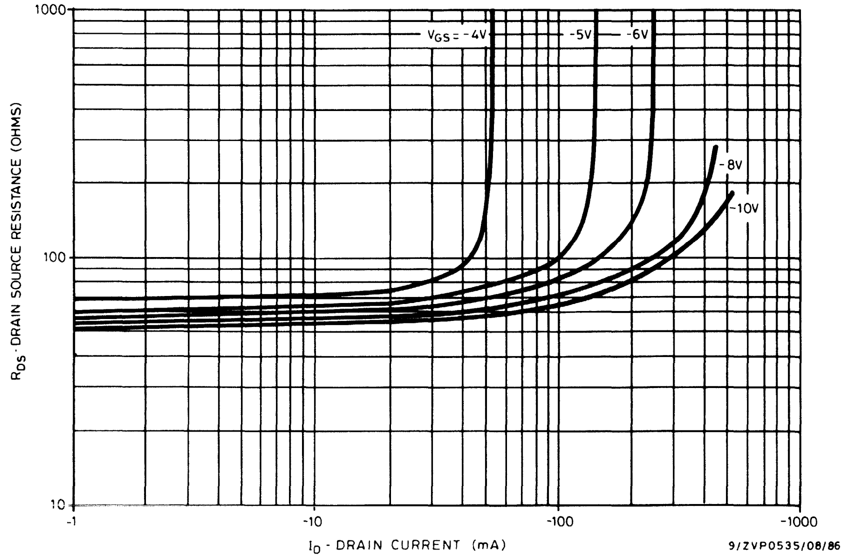


Fig. 9 Typical on-resistance v drain current

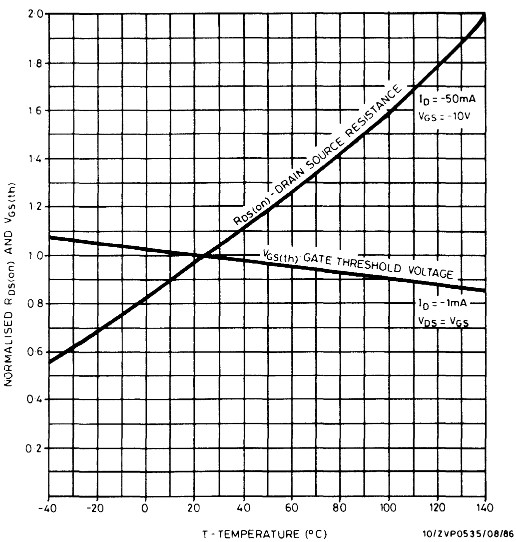


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

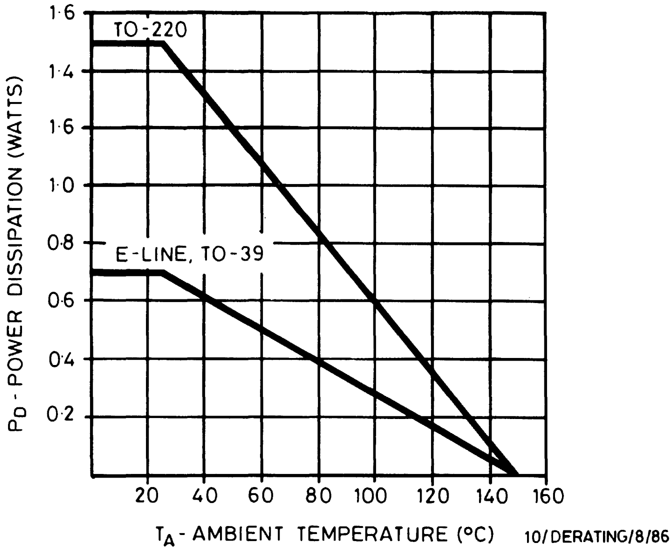


Fig. 11 Power v temperature derating curve (ambient)

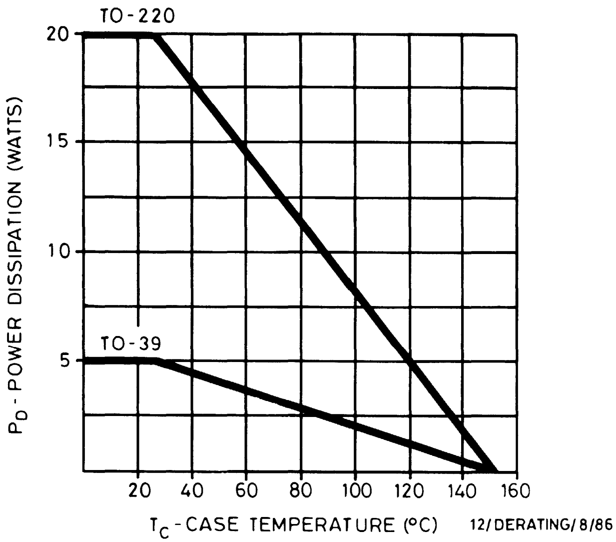


Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

ZVP0540

FEATURES

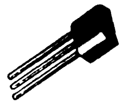
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

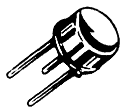
A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

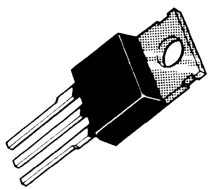
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP0540A	−400V	−0.045A	150Ω
ZVP0540B	−400V	−0.1A	150Ω
ZVP0540L	−400V	−0.1A	150Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVP0540

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	−400	−400	−400	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.045	−0.045	−0.065	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.100	−0.100	A
I_{DM}	Pulse drain current	−0.40	−0.40	−0.40	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−400	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−4.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−20	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−2	mA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−100	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	150	Ω	$I_D = -50mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	40	–	mS	$V_{DS} = -25V$, $I_D = -50mA$
C_{iss}	Input capacitance (2)	–	120	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	10	ns	$V_{DD} \approx -25V$, $I_D = -50mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	15	ns	
t_f	Fall time (2) (3)	–	20	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

P-channel enhancement mode vertical DMOS FET

ZVP0545

FEATURES

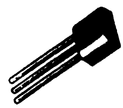
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

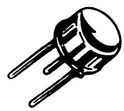
A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

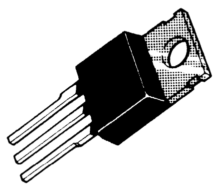
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP0545A	−450V	−0.045A	150Ω
ZVP0545B	−450V	−0.1A	150Ω
ZVP0545L	−450V	−0.1A	150Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVP0545

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	−450	−450	−450	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.045	−0.045	−0.065	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.100	−0.100	A
I_{DM}	Pulse drain current	−0.40	−0.40	−0.40	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−450	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−4.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−20	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−2	mA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−100	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	150	Ω	$I_D = -50mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	40	–	mS	$V_{DS} = -25V$, $I_D = -50mA$
C_{iss}	Input capacitance (2)	–	120	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	20	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	10	ns	$V_{DD} \approx -25V$, $I_D = -50mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	15	ns	
t_f	Fall time (2) (3)	–	20	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

P-channel enhancement mode vertical DMOS FET

ZVP1320

FEATURES

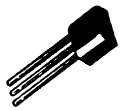
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

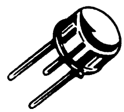
A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

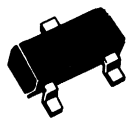
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP1320A	−200V	−0.07A	80Ω
ZVP1320B	−200V	−0.10A	80Ω
ZVP1320F	−200V	−0.035A	80Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



SOT-23
SUFFIX F

ZVP1320

ABSOLUTE MAXIMUM RATINGS

Parameters		E-line	TO-39	SOT-23	Units
V_{DS}	Drain-source voltage	−200	−200	−200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.07	−0.07	−0.035	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.10	–	A
I_{DM}	Pulse drain current	−0.4	−0.4	−0.4	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.625	0.25	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

Parameter		Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−200	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−100	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	80	Ω	$I_D = -50mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	25	–	mS	$V_{DS} = -25V$, $I_D = -50mA$
C_{iss}	Input capacitance (2)	–	50	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	15	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx -25V$, $I_D = -50mA$
t_r	Rise time (2) (3)	–	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	ns	
t_f	Fall time (2) (3)	–	16	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

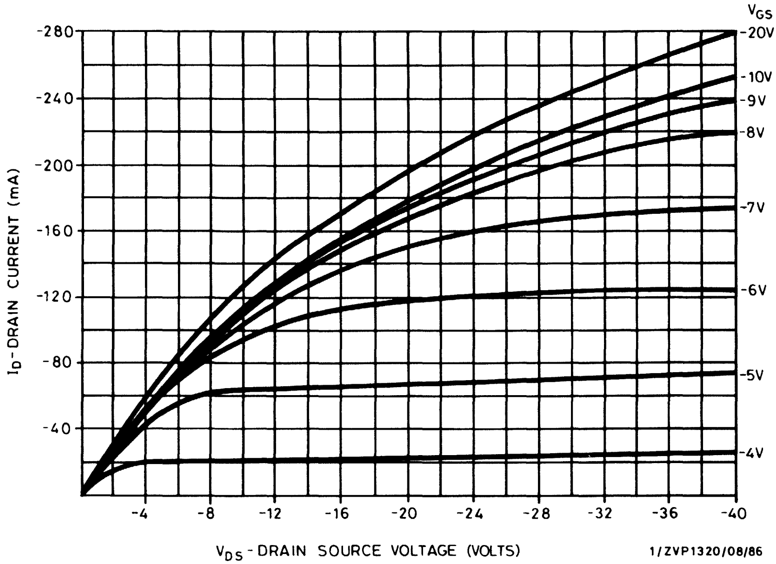


Fig. 1 Typical output characteristics

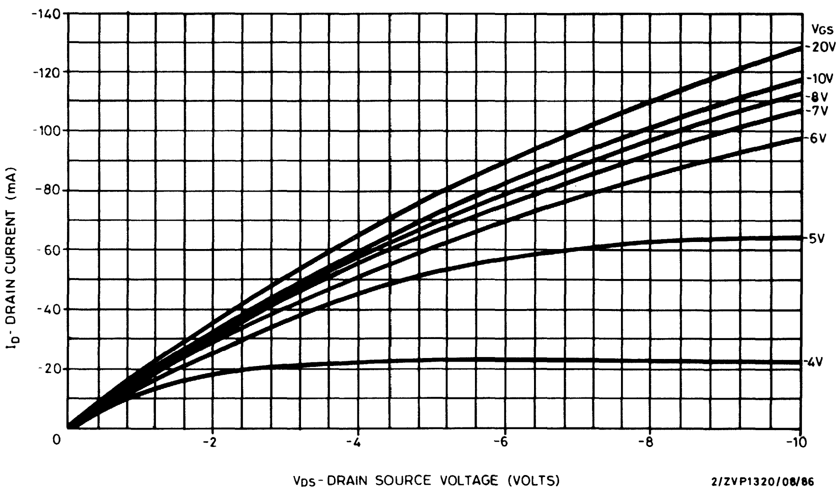


Fig. 2 Typical saturation characteristics

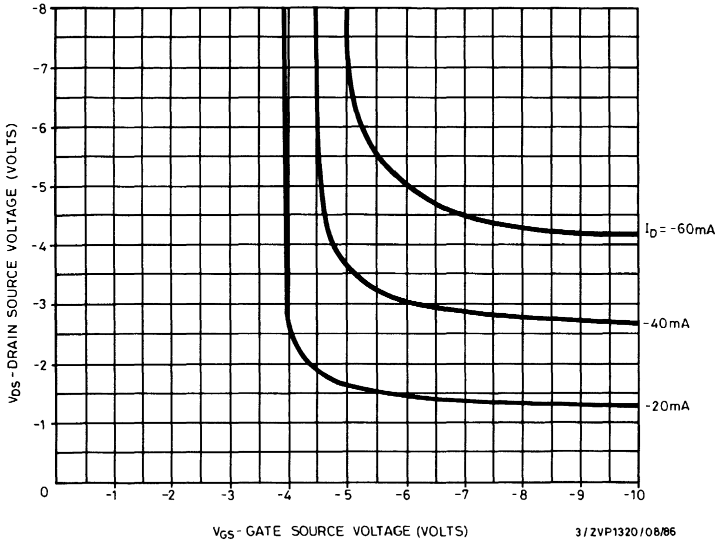


Fig. 3 Typical voltage saturation characteristics

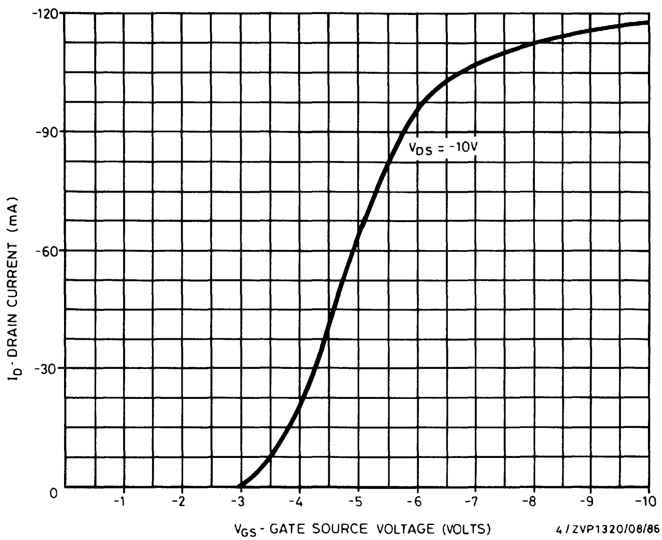


Fig. 4 Typical transfer characteristics

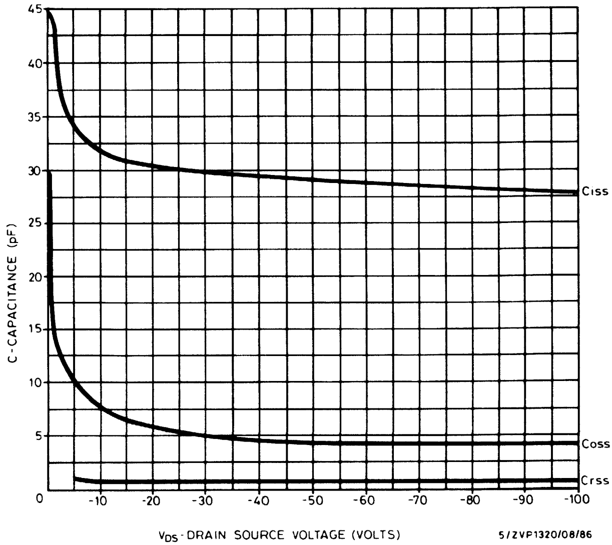


Fig. 5 Typical capacitance v drain-source voltage

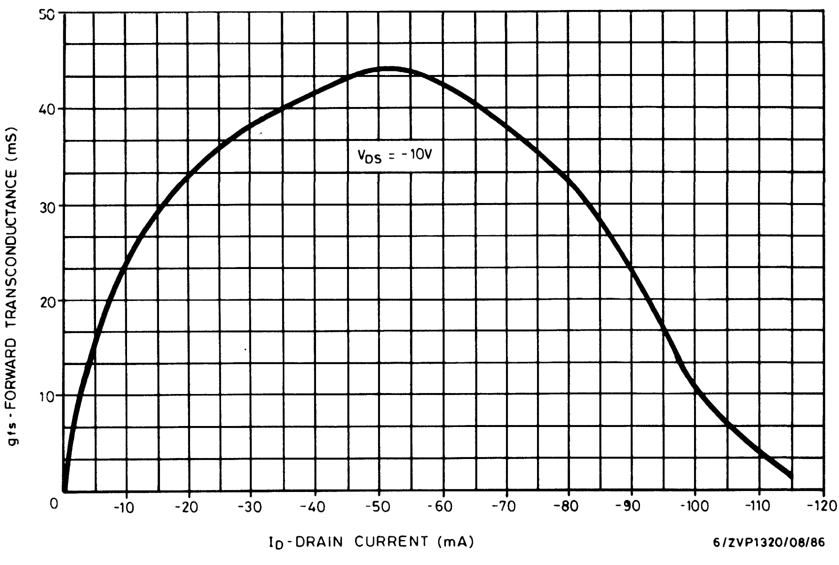


Fig. 6 Typical transconductance v drain current

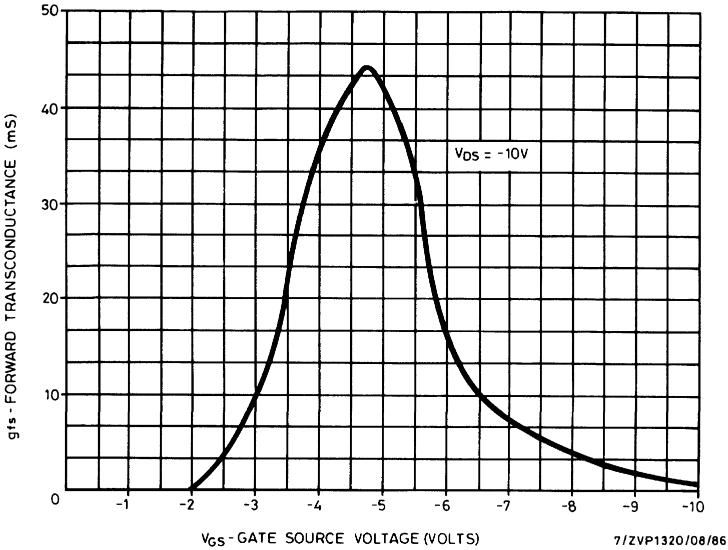


Fig. 7 Typical transconductance v gate-source voltage

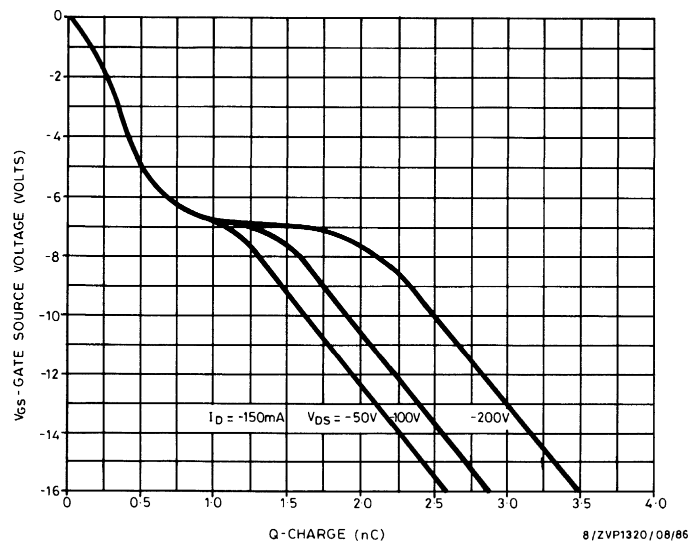


Fig. 8 Typical gate charge v gate-source voltage

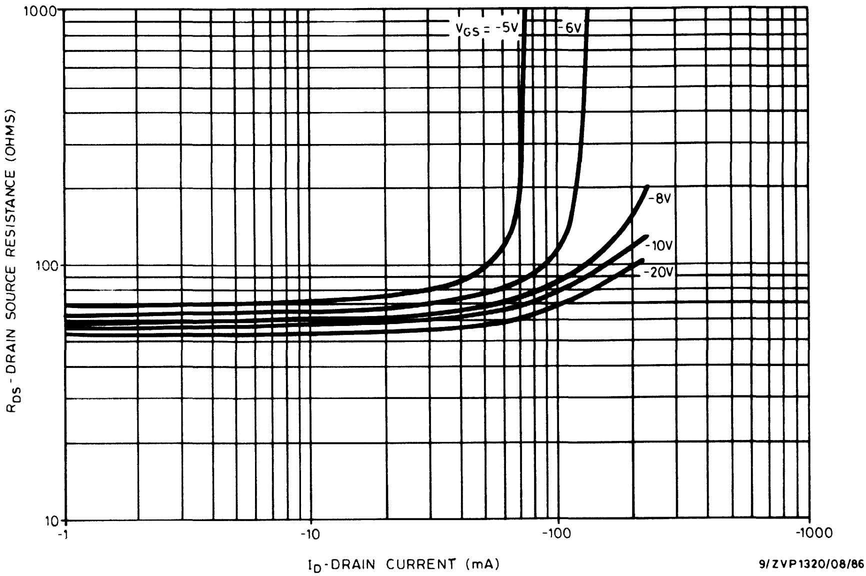


Fig. 9 Typical on-resistance v drain current

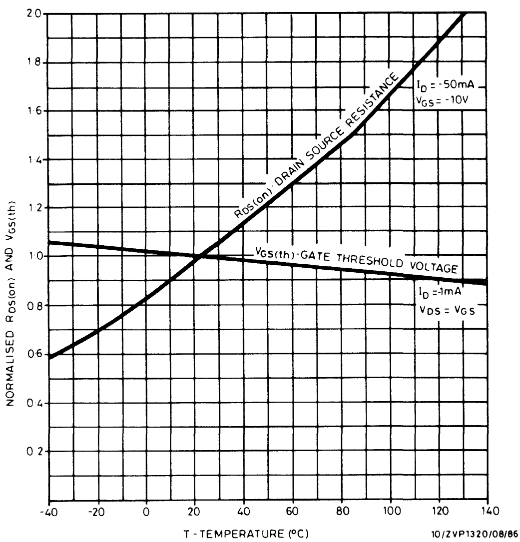


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

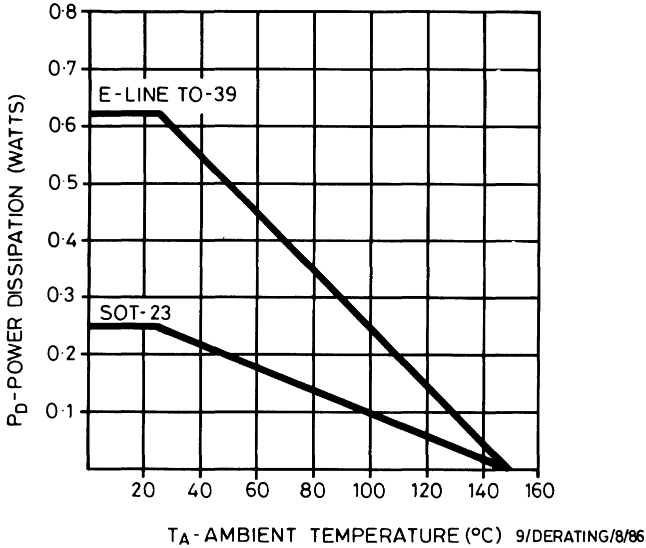


Fig. 11 Power v temperature derating curve (ambient)

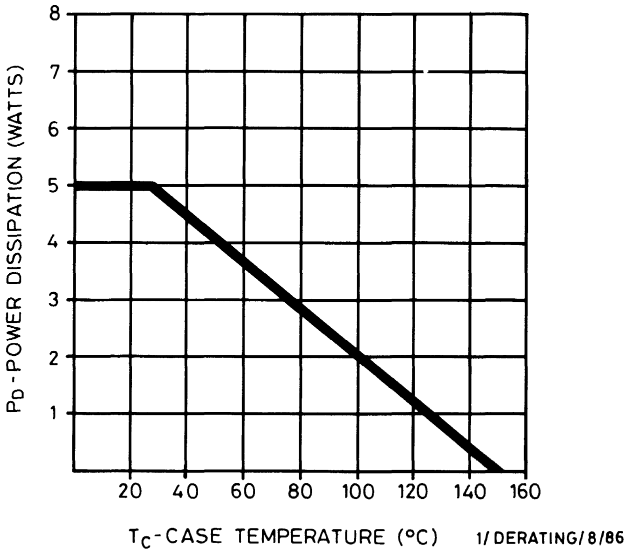


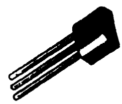
Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

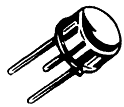
ZVP2106

FEATURES

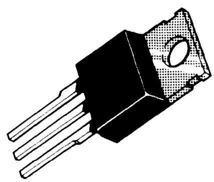
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP2106A*	−60V	−0.28A	5Ω
ZVP2106B*	−60V	−0.76A	5Ω
ZVP2106L	−60V	−1.0A	5Ω

*BS-CECC approved

ZVP2106

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	-60	-60	-60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	-0.28	-0.28	-0.38	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	-0.76	-1.0	A
I_{DM}	Pulsed drain current	-4	-4	-4	A
V_{GS}	Gate-source voltage	± 20	± 20	± 20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	-55 to $+150$			°C

ELECTRICAL CHARACTERISTICS (at $T = 25°C$ unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	-60	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	-1.5	-3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	-0.5	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	-100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	-1	–	A	$V_{DS} = -18V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	5	Ω	$I_D = -500mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	150	–	mS	$V_{DS} = -18V$, $I_D = -500mA$
C_{iss}	Input capacitance (2)	–	100	pF	$V_{DS} = -18V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	60	pF	
C_{rss}	Reverse transfer capacitance (2)	–	20	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx -18V$, $I_D = -500mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

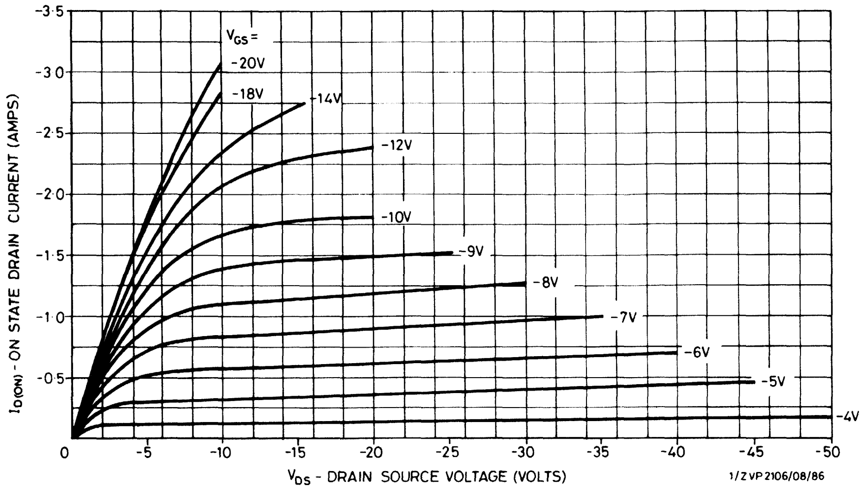


Fig. 1 Typical output characteristics

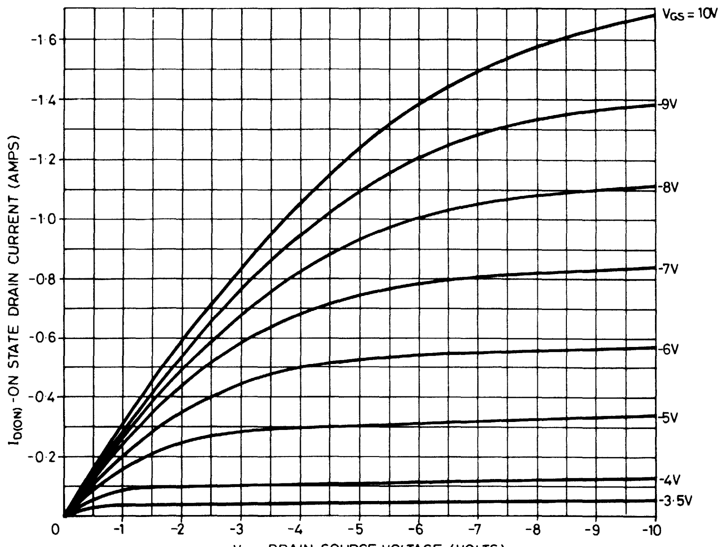


Fig. 2 Typical saturation characteristics

ZVP2106

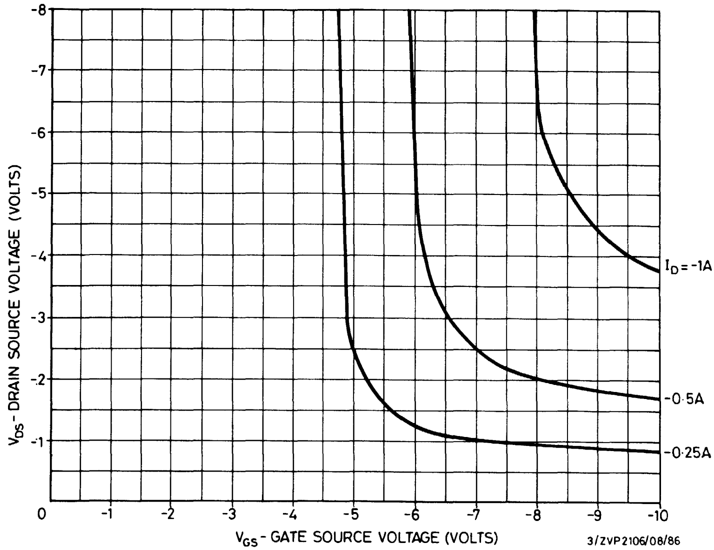


Fig. 3 Typical voltage saturation characteristics

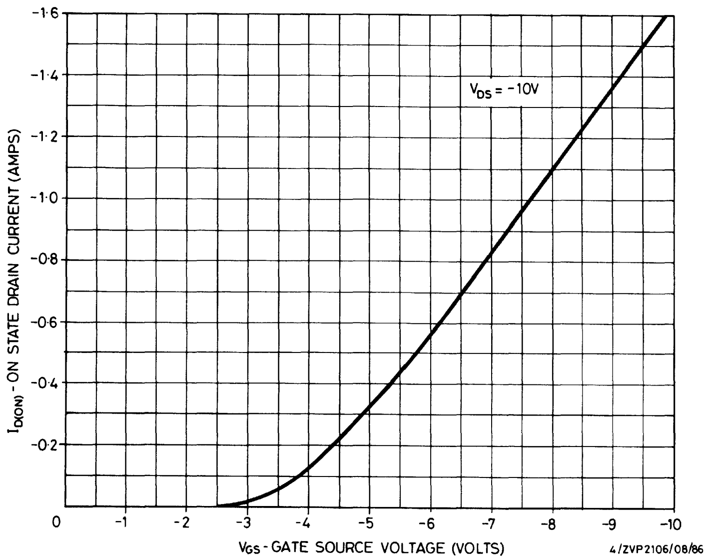


Fig. 4 Typical transfer characteristics

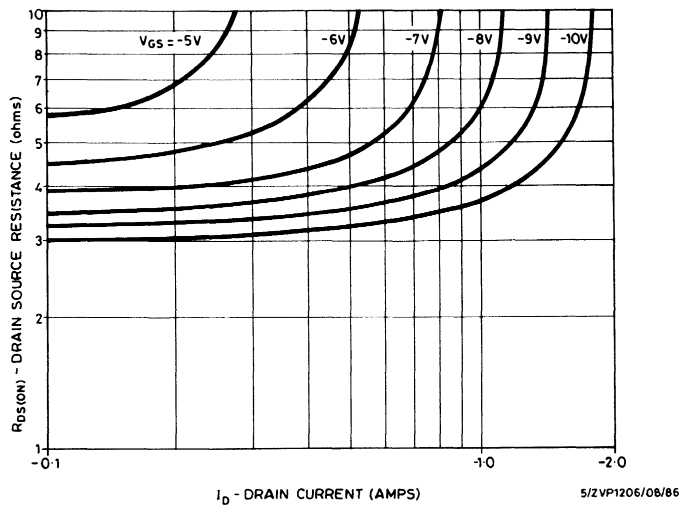


Fig. 5 Typical on-resistance v drain current

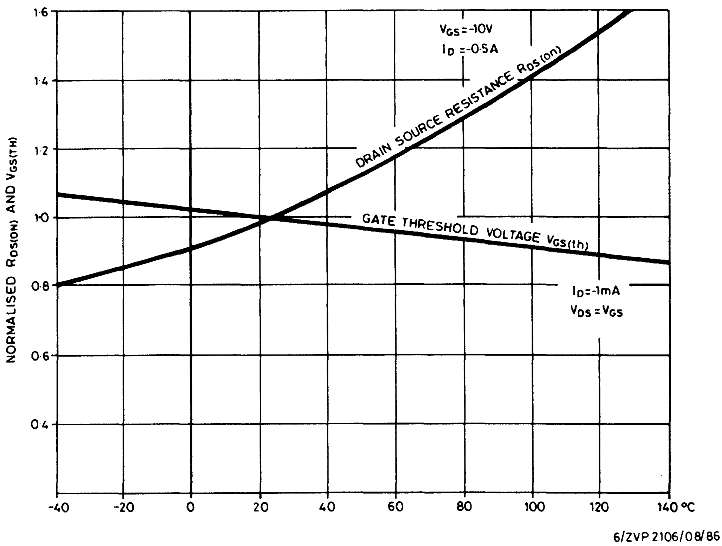


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

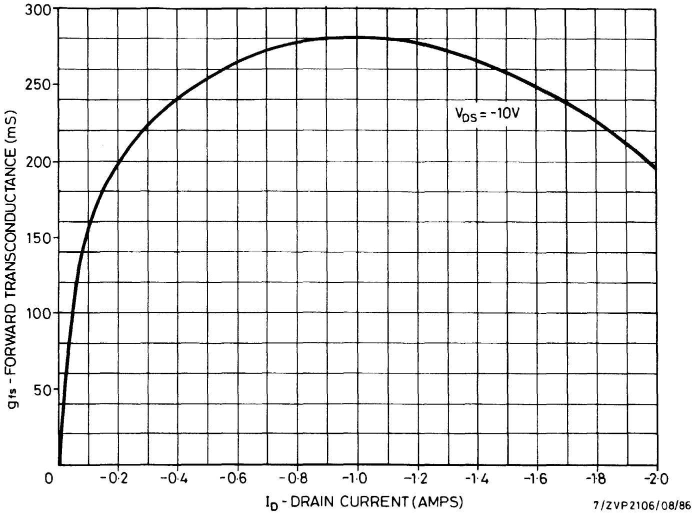


Fig. 7 Typical transconductance v drain current

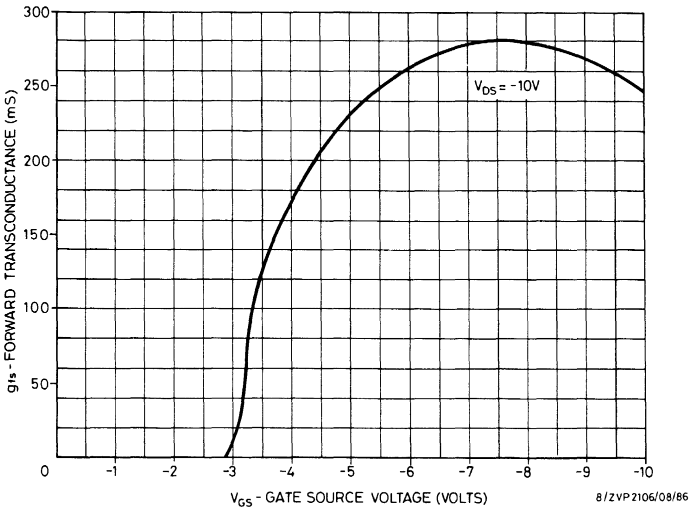


Fig. 8 Typical transconductance v gate-source voltage

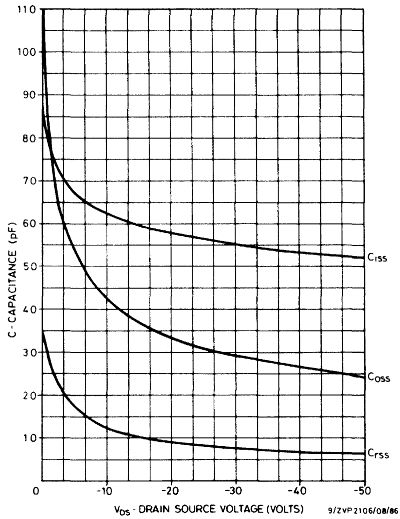


Fig. 9 Typical capacitance v drain-source voltage

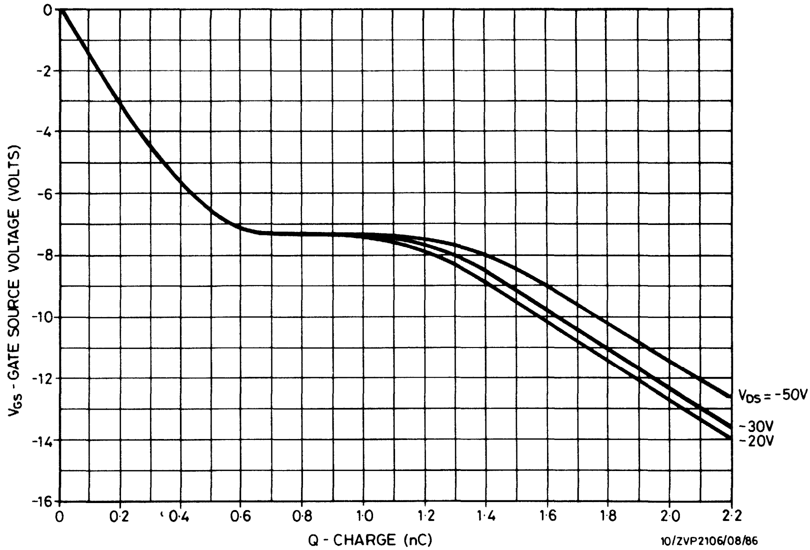


Fig. 10 Typical gate charge v gate-source voltage

ZVP2106

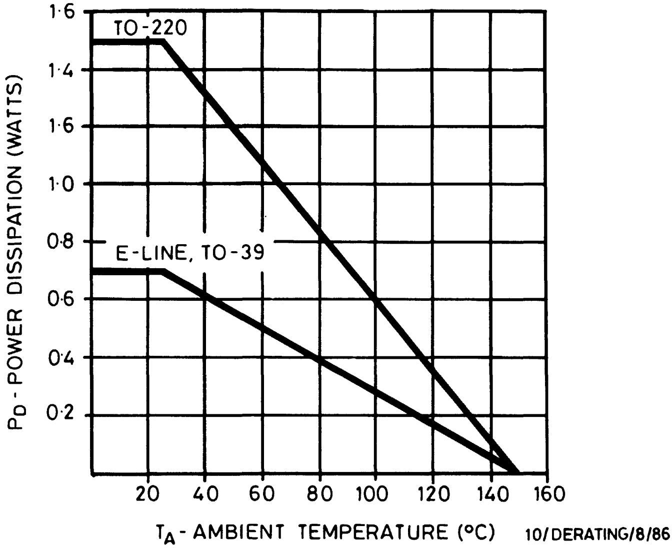


Fig. 11 Power v temperature derating curve (ambient)

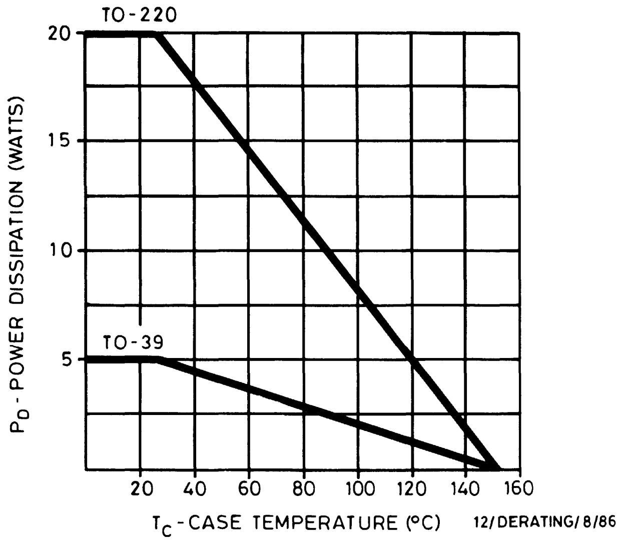


Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

ZVP2110

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

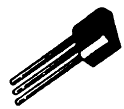
DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

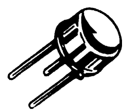
PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP2110A*	−100V	−0.23A	8Ω
ZVP2110B*	−100V	−0.60A	8Ω
ZVP2110L	−100V	−0.75A	8Ω

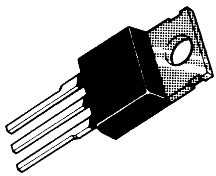
*BS-CECC approved



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVP2110

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	−100	−100	−100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.23	−0.23	−0.30	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.60	−0.75	A
I_{DM}	Pulsed drain current	−3	−3	−3	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−100	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−1	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−750	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	8	Ω	$I_D = -375mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	125	–	mS	$V_{DS} = -25V$, $I_D = -375mA$
C_{iss}	Input capacitance (2)	–	100	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	35	pF	
C_{rss}	Reverse transfer capacitance (2)	–	10	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx -25V$, $I_D = -375mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

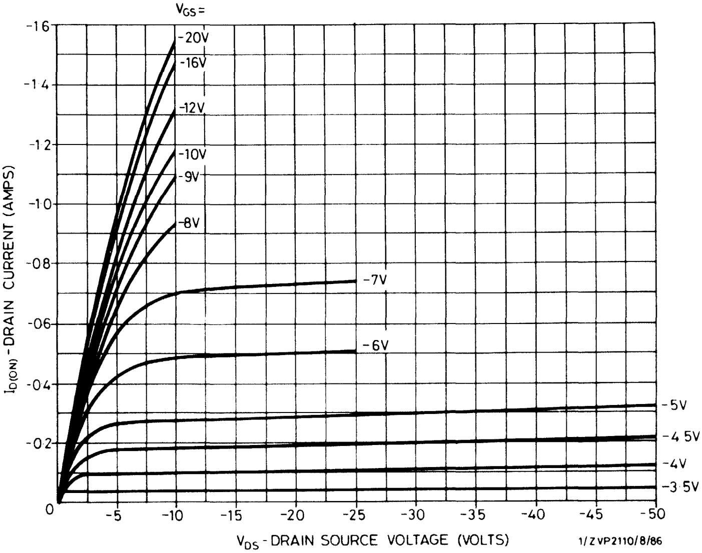


Fig. 1 Typical output characteristics

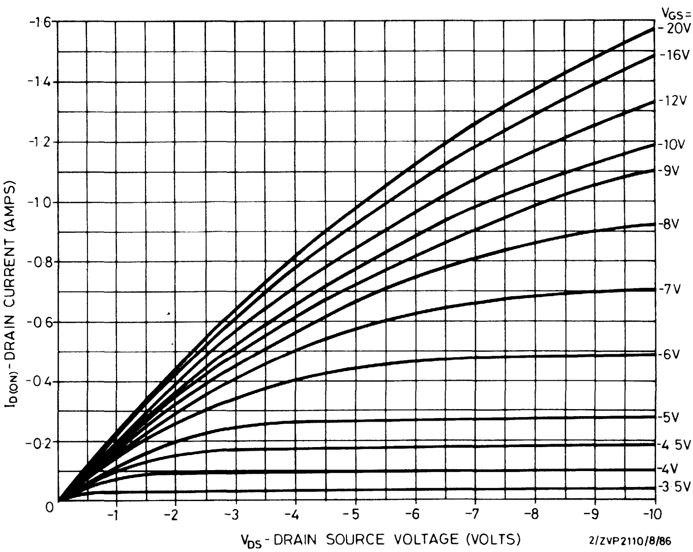


Fig. 2 Typical saturation characteristics

ZVP2110

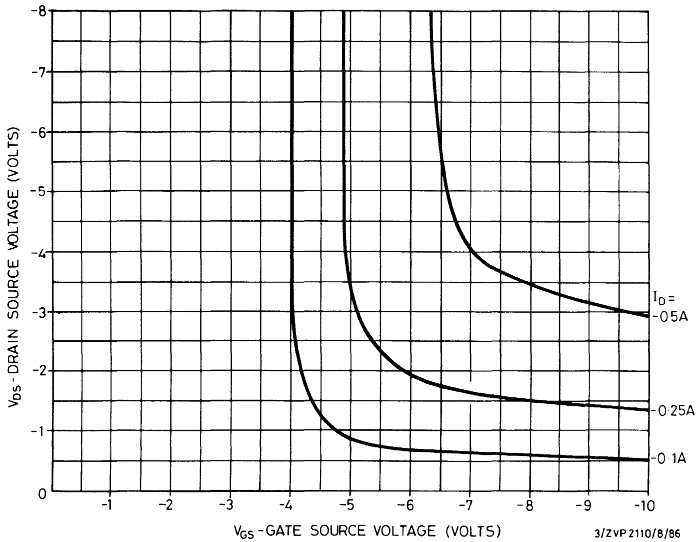


Fig. 3 Typical voltage saturation characteristics

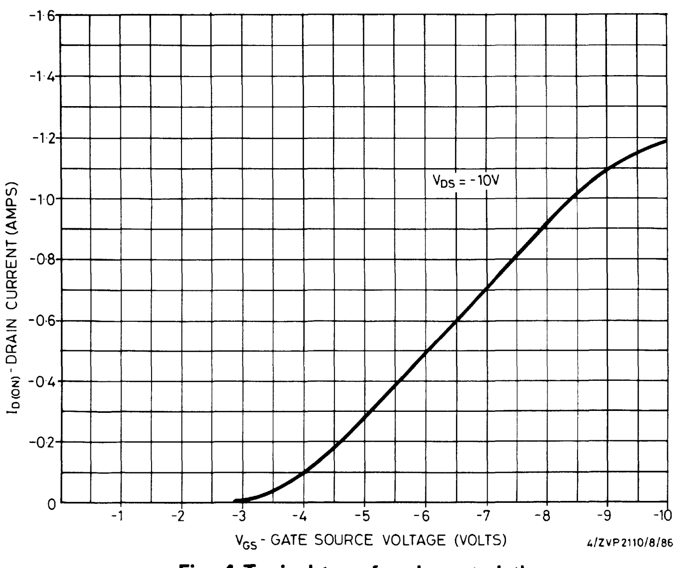


Fig. 4 Typical transfer characteristics

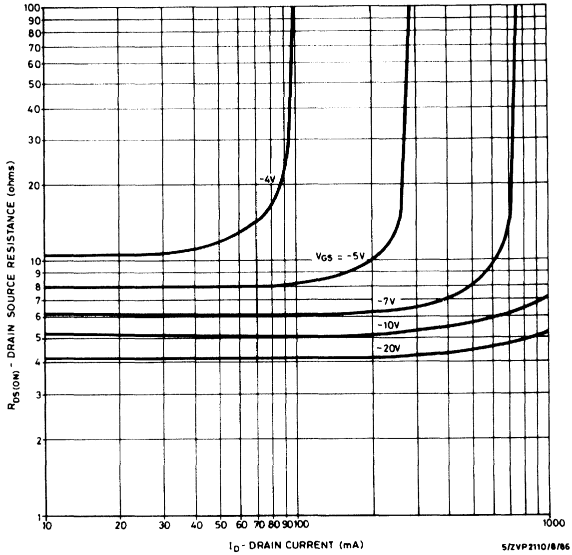


Fig. 5 Typical on-resistance v drain current

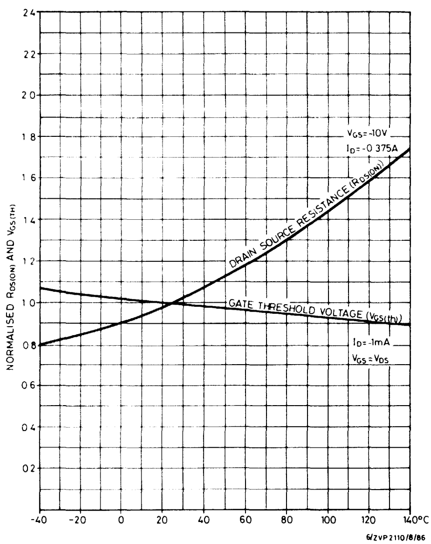


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

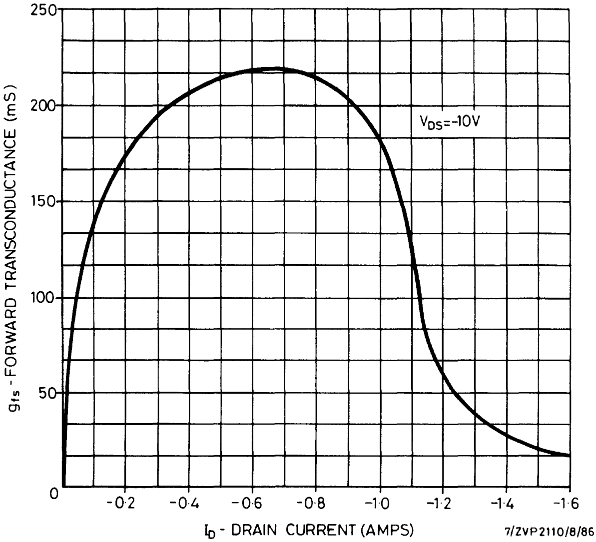


Fig. 7 Typical transconductance v drain current

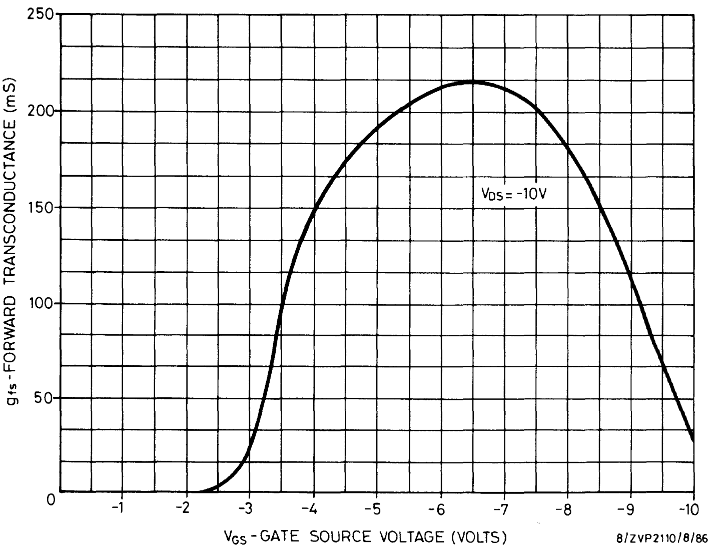


Fig. 8 Typical transconductance v gate-source voltage

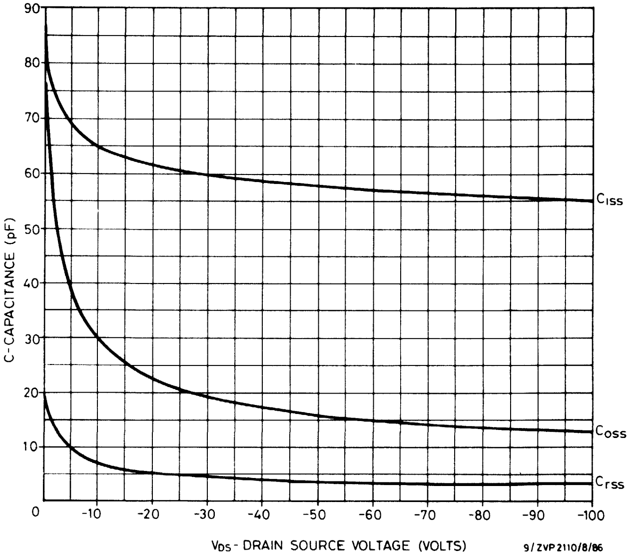


Fig. 9 Typical capacitance v drain-source voltage

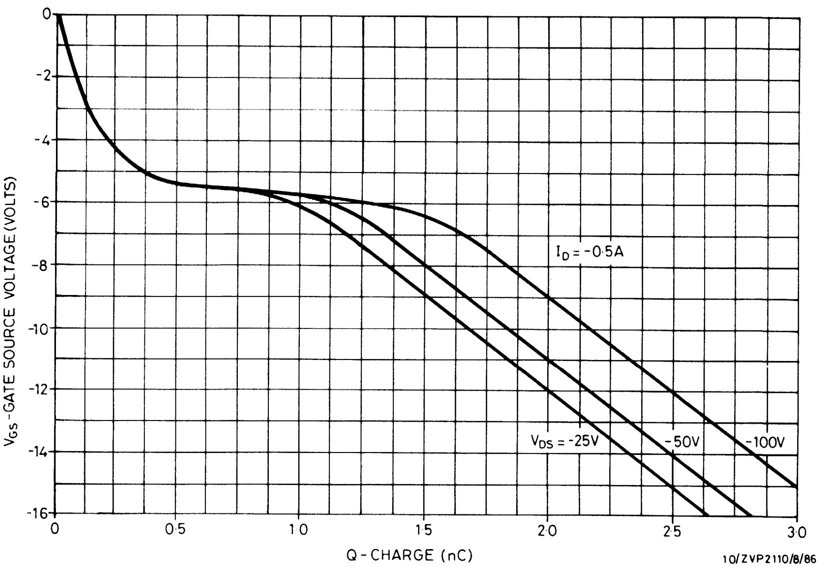


Fig. 10 Typical gate charge v gate-source voltage

ZVP2110

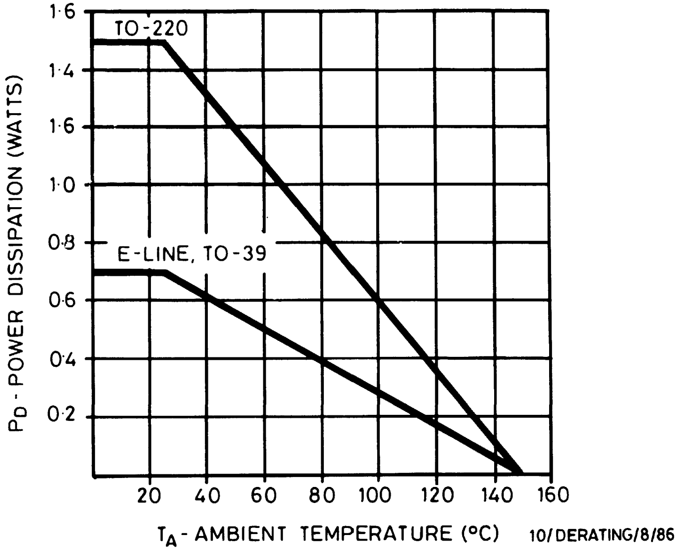


Fig. 11 Power v temperature derating curve (ambient)

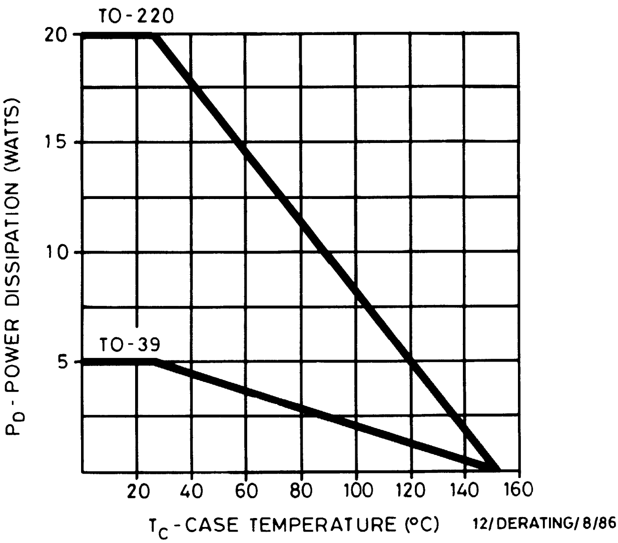


Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

ZVP2120

FEATURES

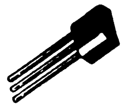
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

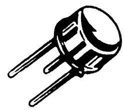
A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

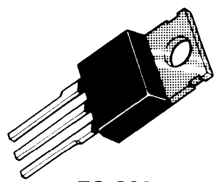
Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP2120A	−200V	−0.12A	25Ω
ZVP2120B	−200V	−0.3A	25Ω
ZVP2120L	−200V	−0.3A	25Ω



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



TO-220
SUFFIX L

ZVP2120

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	−200	−200	−200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.12	−0.12	−0.16	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.3	−0.3	A
I_{DM}	Pulsed drain current	−1.2	−1.2	−1.2	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−200	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−100	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−300	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	25	Ω	$I_D = -150mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	50	–	mS	$V_{DS} = -25V$, $I_D = -150mA$
C_{iss}	Input capacitance (2)	–	100	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	7	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	7	ns	$V_{DD} \approx -25V$, $I_D = -150mA$
t_r	Rise time (2) (3)	–	15	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	12	ns	
t_f	Fall time (2) (3)	–	15	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

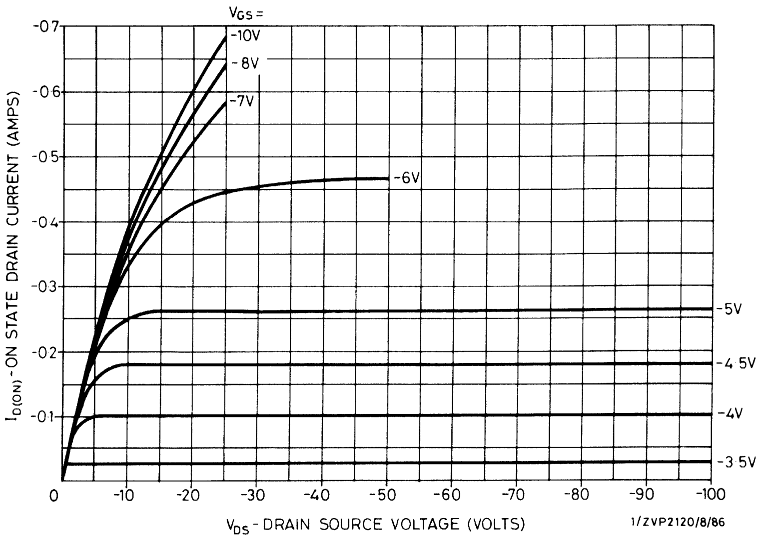


Fig. 1 Typical output characteristics

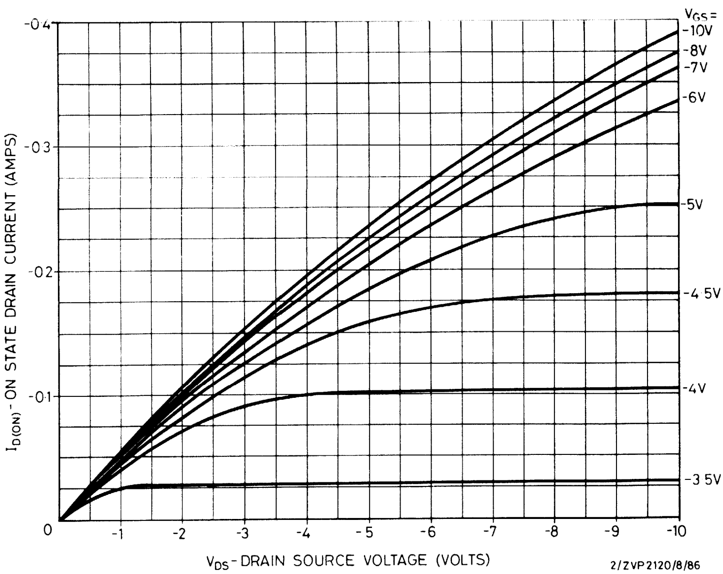


Fig. 2 Typical saturation characteristics

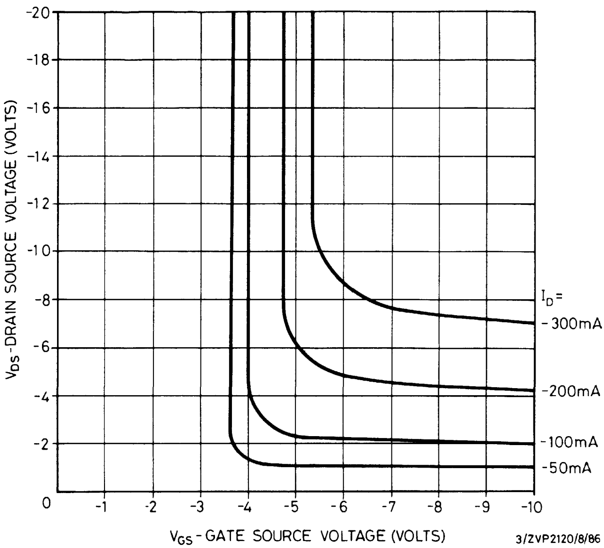


Fig. 3 Typical voltage saturation characteristics

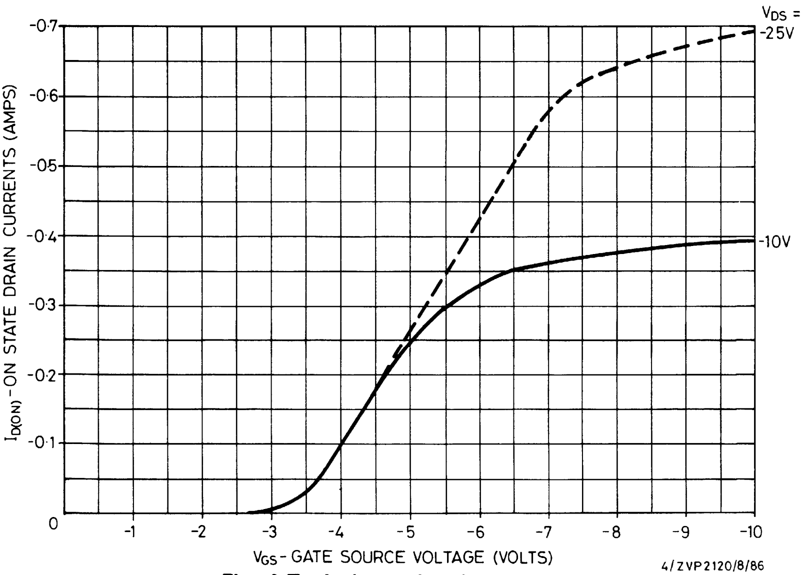


Fig. 4 Typical transfer characteristics

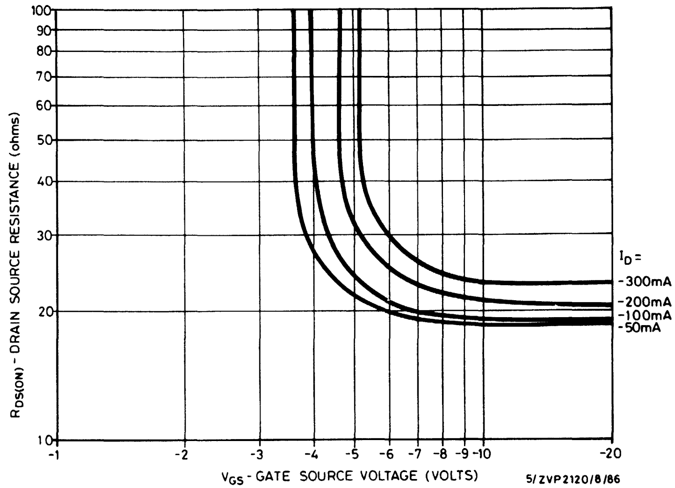


Fig. 5 Typical on-resistance v gate-source voltage

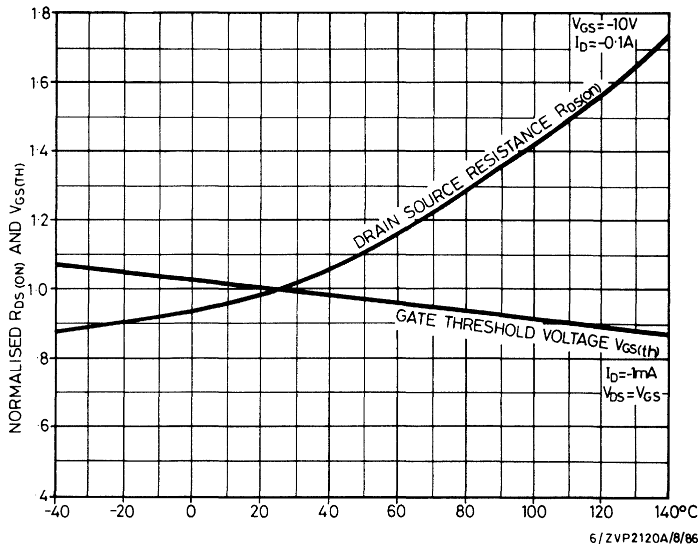


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

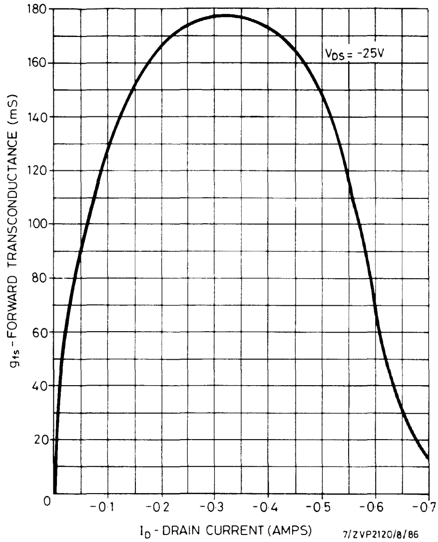


Fig. 7 Typical transconductance v drain current

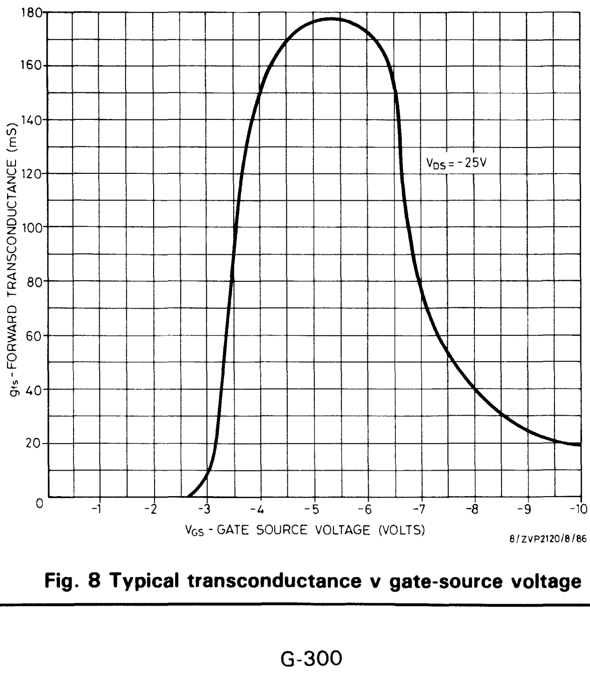


Fig. 8 Typical transconductance v gate-source voltage

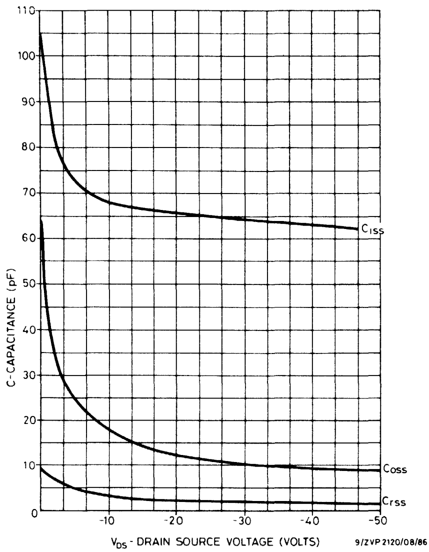


Fig. 9 Typical capacitance v drain-source voltage

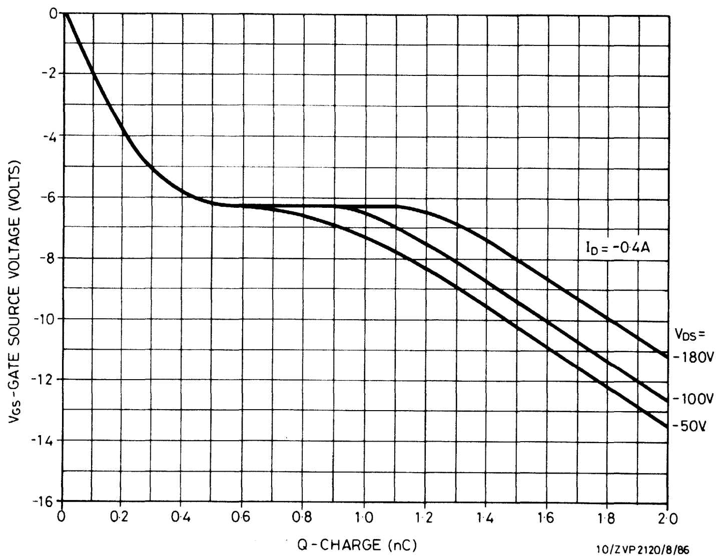


Fig. 10 Typical gate charge v gate-source voltage

ZVP2120

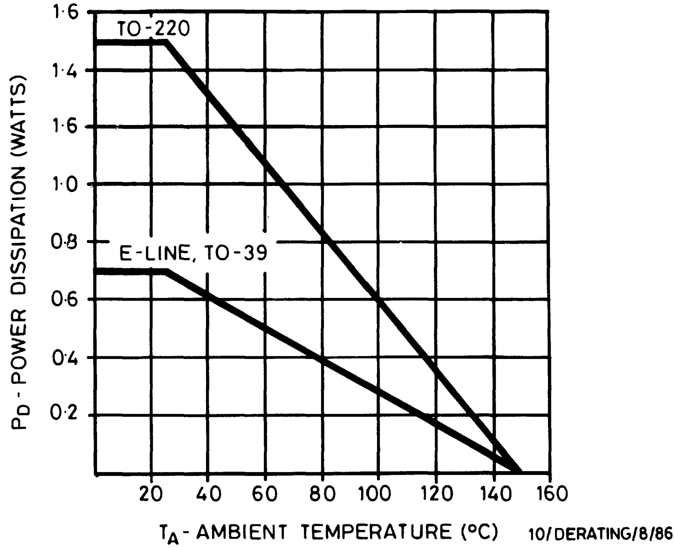


Fig. 11 Power v temperature derating curve (ambient)

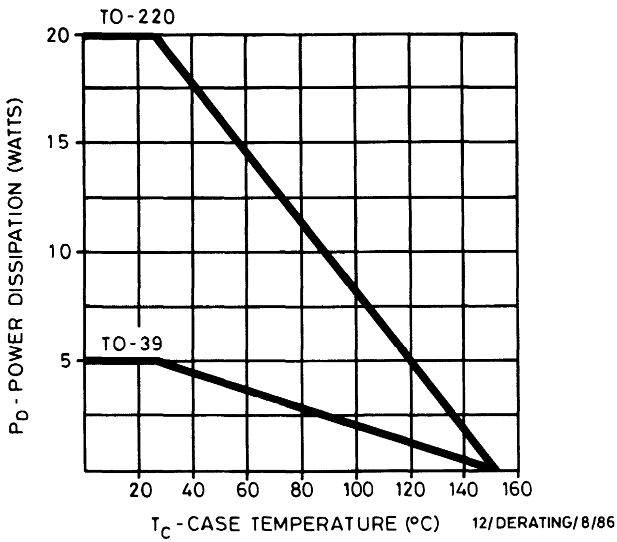


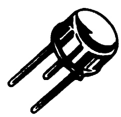
Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

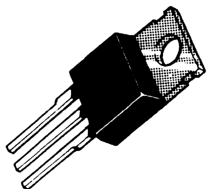
ZVP2206

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-39
SUFFIX B



TO-220
SUFFIX L

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP2206B*	−60V	−2.0A	1.6Ω
ZVP2206L	−60V	−2.0A	1.6Ω

*BS-CECC approved

ZVP2206

ABSOLUTE MAXIMUM RATINGS

	Parameters	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	−60	−60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.5	−0.75	A
I_D	Continuous drain current (@ $T_C = 25°C$)	−2	−2	A
I_{DM}	Pulse drain current	−8	−8	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	20	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−60	–	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	–	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	−2	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	−200	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−2	–	–	A	$V_{DS} = -18V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	1.6	Ω	$I_D = -1A$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	–	600	–	mS	$V_{DS} = -18V$, $I_D = -1A$
C_{iss}	Input capacitance (2)	–	–	240	pF	$V_{DS} = -18V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–		150	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	40	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	–	10	ns	$V_{DD} \approx -18V$, $I_D = -1A$
t_r	Rise time (2) (3)	–	–	20	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	–	25	ns	
t_f	Fall time (2) (3)	–	–	20	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

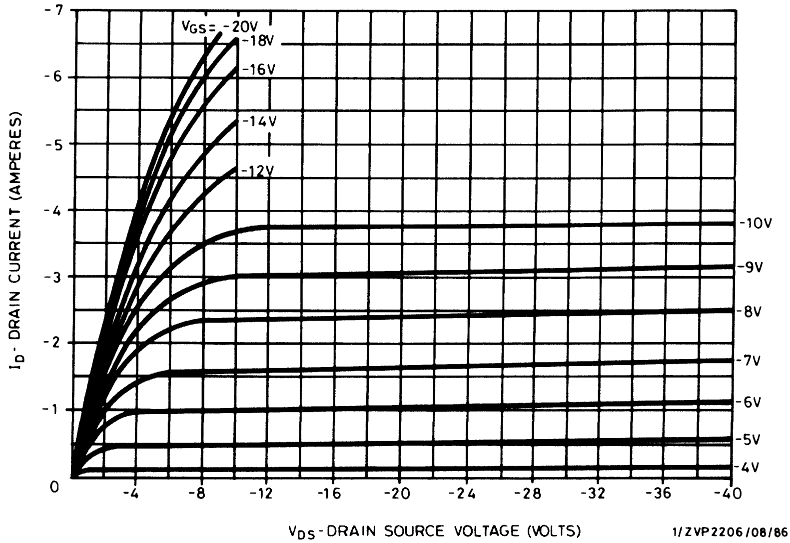


Fig. 1 Typical output characteristics

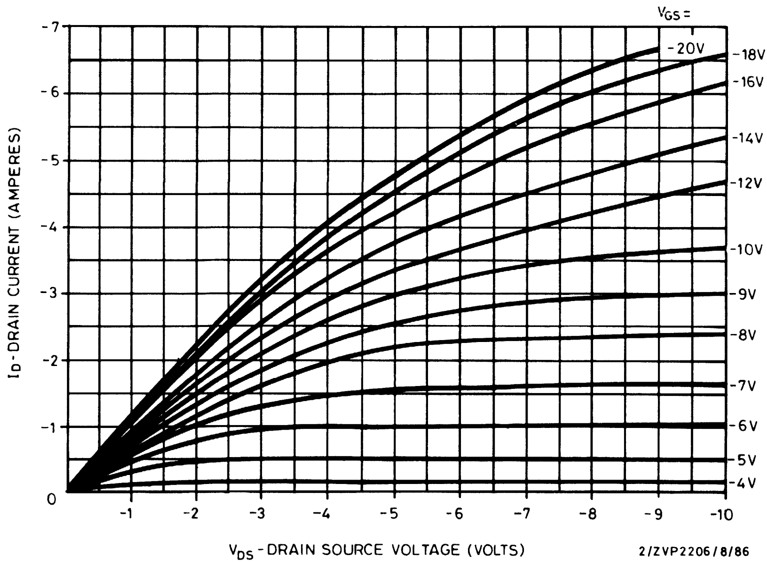


Fig. 2 Typical saturation characteristics

ZVP2206

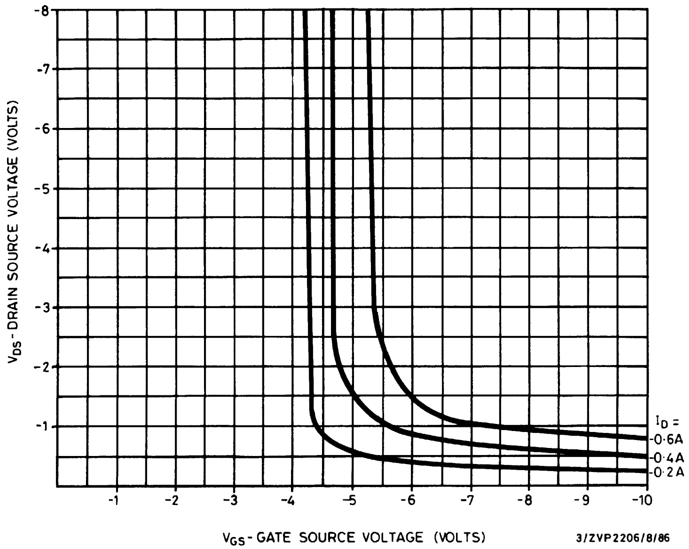


Fig. 3 Typical voltage saturation characteristics

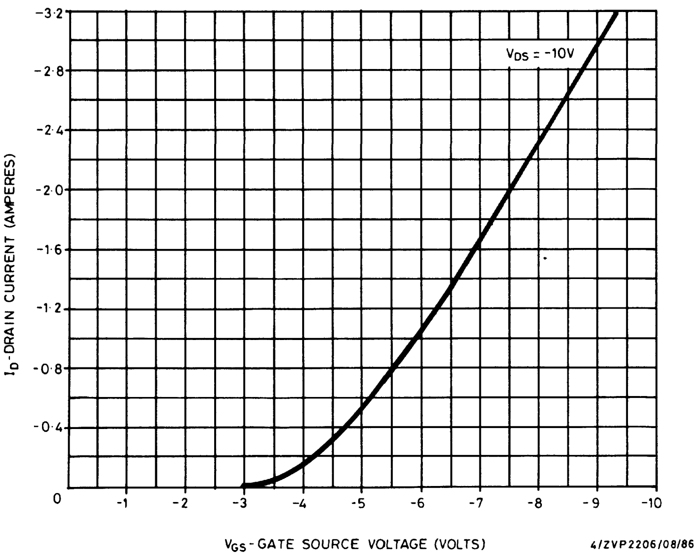


Fig. 4 Typical transfer characteristics

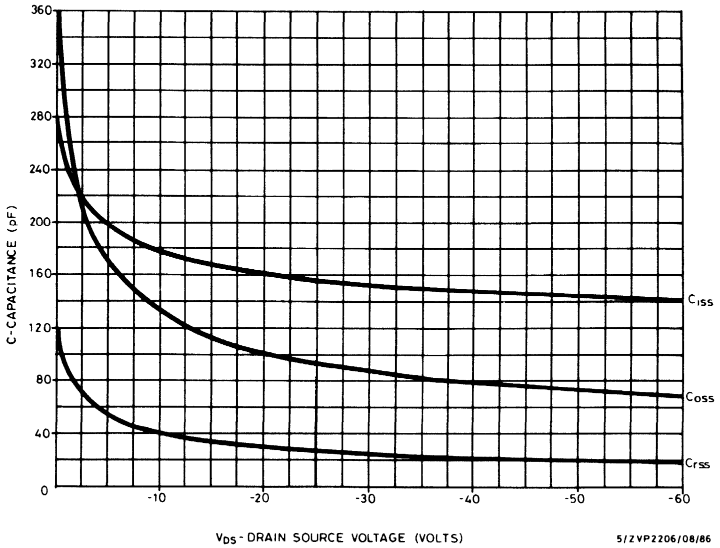


Fig. 5 Typical capacitance v drain-source voltage

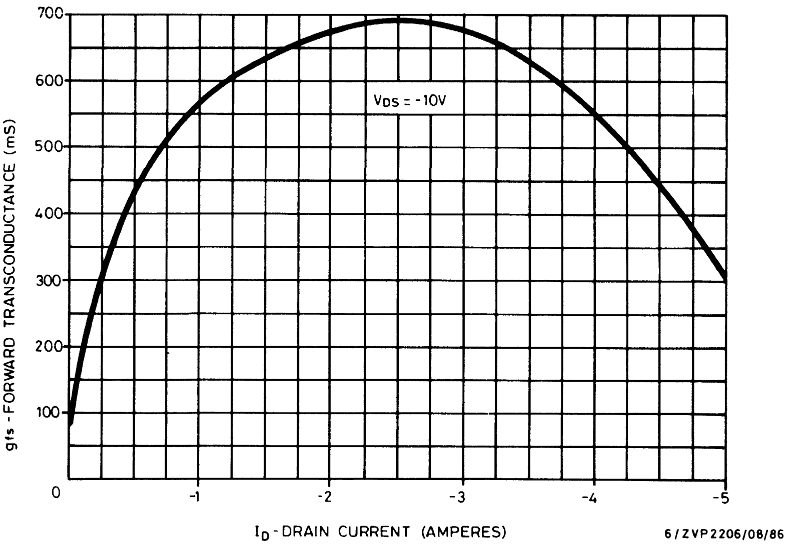


Fig. 6 Typical transconductance v drain current

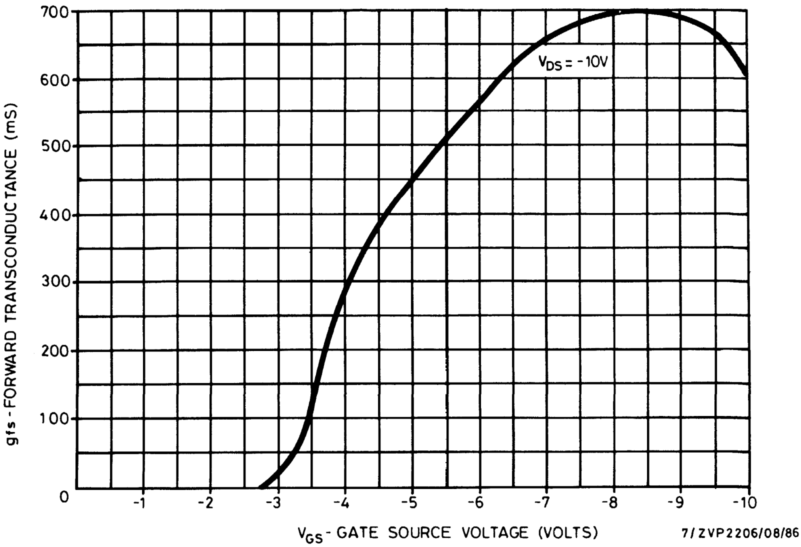


Fig. 7 Typical transconductance v gate-source voltage

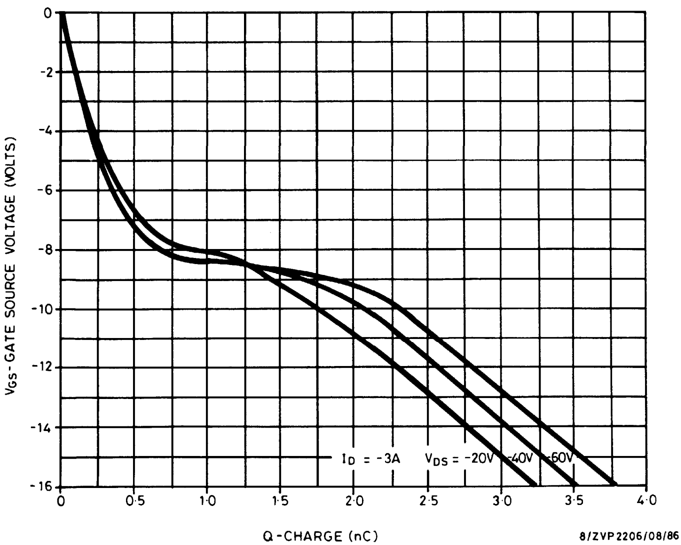


Fig. 8 Typical gate charge v gate-source voltage

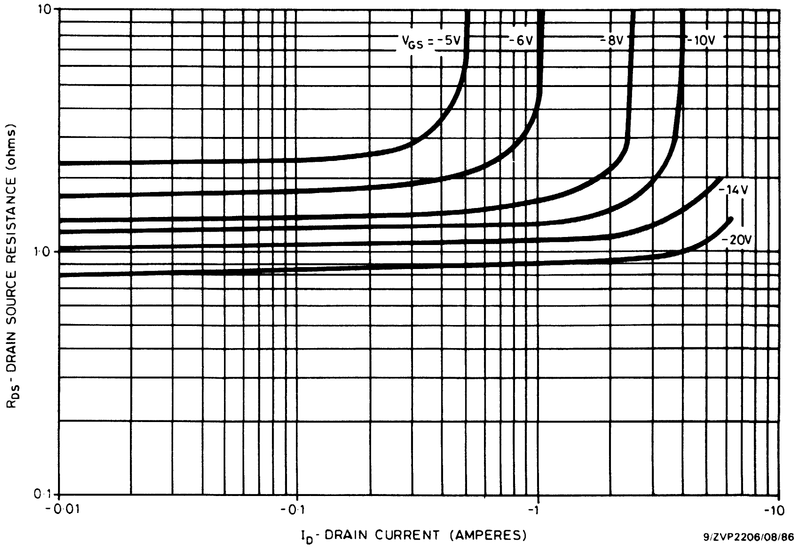


Fig. 9 Typical on-resistance v drain current

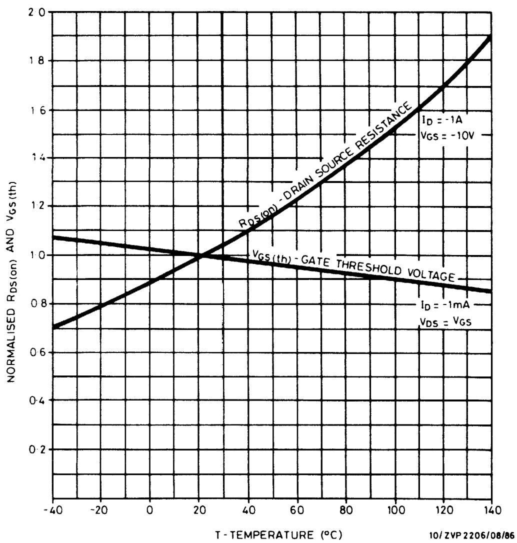


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

ZVP2206

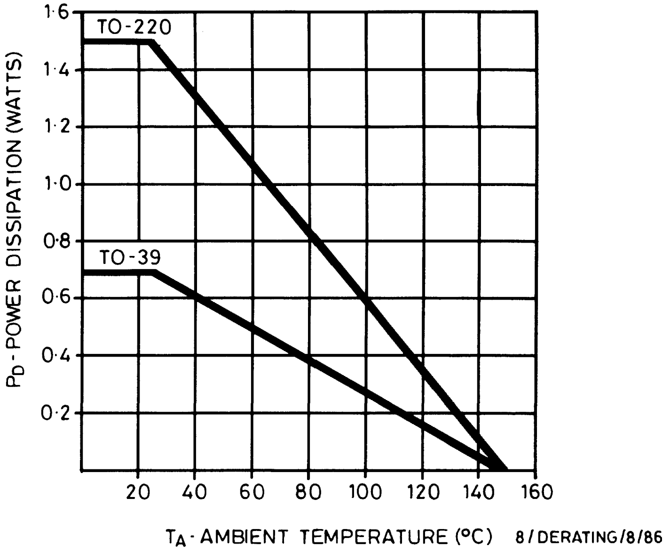


Fig. 11 Power v temperature derating curve (ambient)

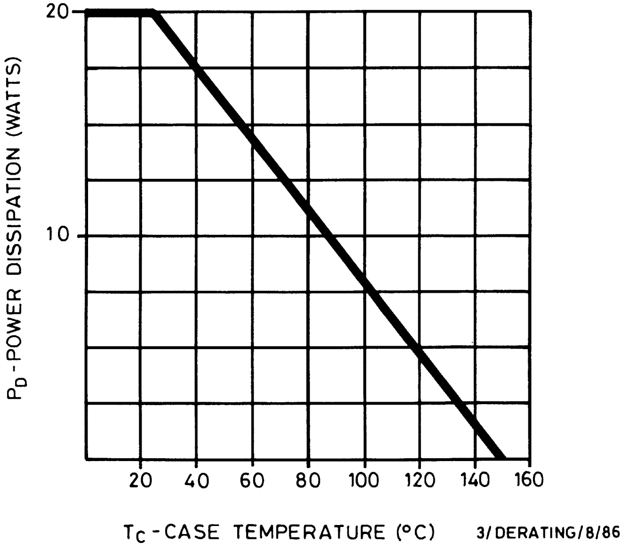


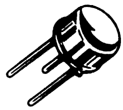
Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

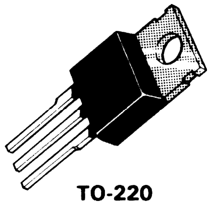
ZVP2210

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



TO-39
SUFFIX B



TO-220
SUFFIX L

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP2210B*	– 100V	– 1.5A	3Ω
ZVP2210L	– 100V	– 1.5A	3Ω

*BS-CECC approved

ZVP2210

ABSOLUTE MAXIMUM RATINGS

	Parameters	TO-39	TO-220	Units
V_{DS}	Drain-source voltage	−100	−100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.33	−0.48	A
I_D	Continuous drain current (@ $T_C = 25°C$)	−1.5	−1.5	A
I_{DM}	Pulse drain current	−6	−6	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	20	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−100	–	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	–	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	−2	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	−200	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−1.5	–	–	A	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	3	Ω	$I_D = -750mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	–	500	–	mS	$V_{DS} = -25V$, $I_D = -750mA$
C_{iss}	Input capacitance (2)	–	–	240	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–		100	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	25	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	–	10	ns	$V_{DD} \approx -25V$, $I_D = -750mA$
t_r	Rise time (2) (3)	–	–	20	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	–	25	ns	
t_f	Fall time (2) (3)	–	–	20	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ⩽2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

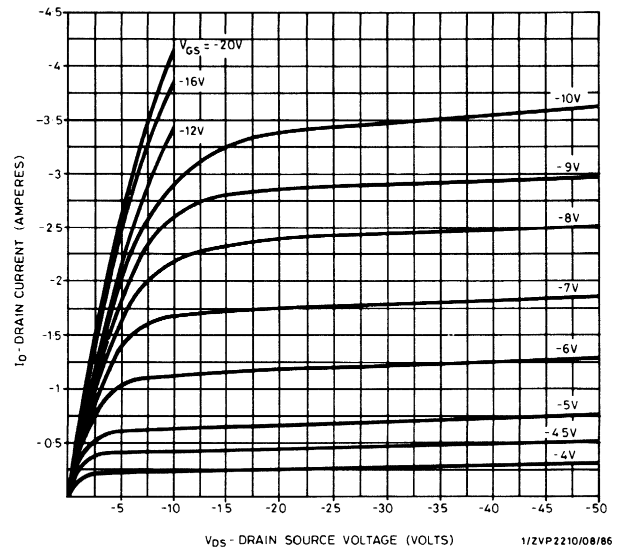


Fig. 1 Typical output characteristics

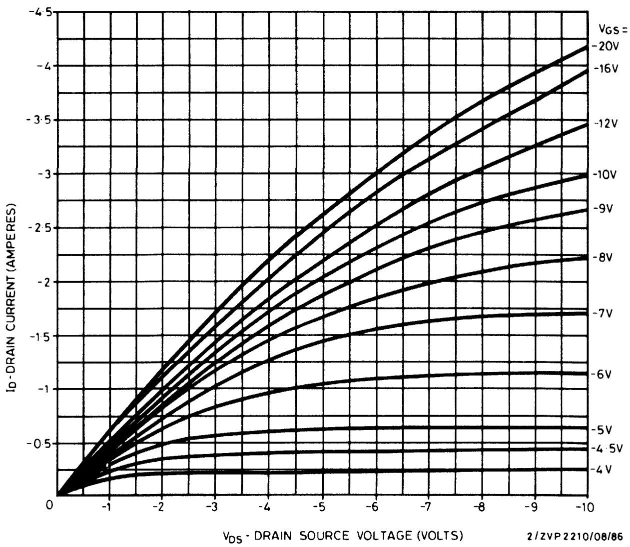


Fig. 2 Typical saturation characteristics

ZVP2210

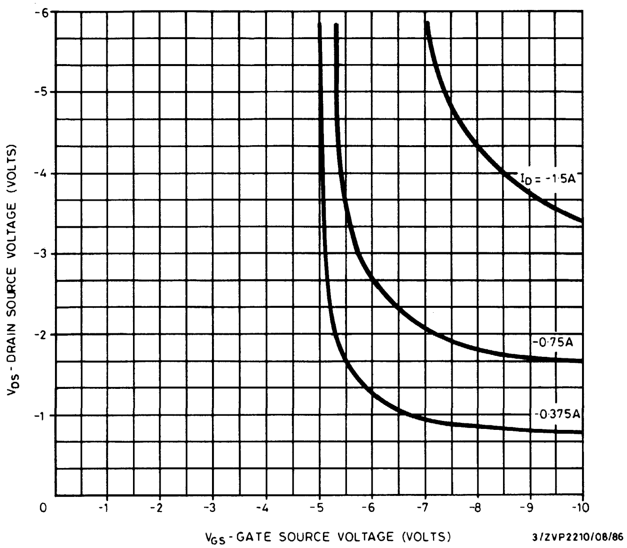


Fig. 3 Typical voltage saturation characteristics

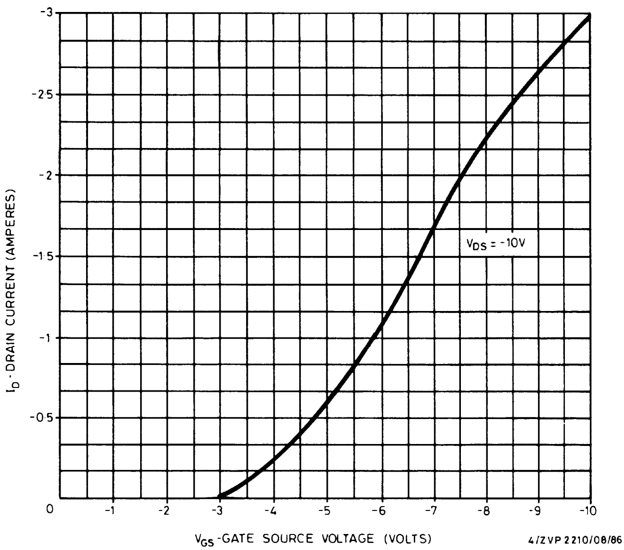


Fig. 4 Typical transfer characteristics

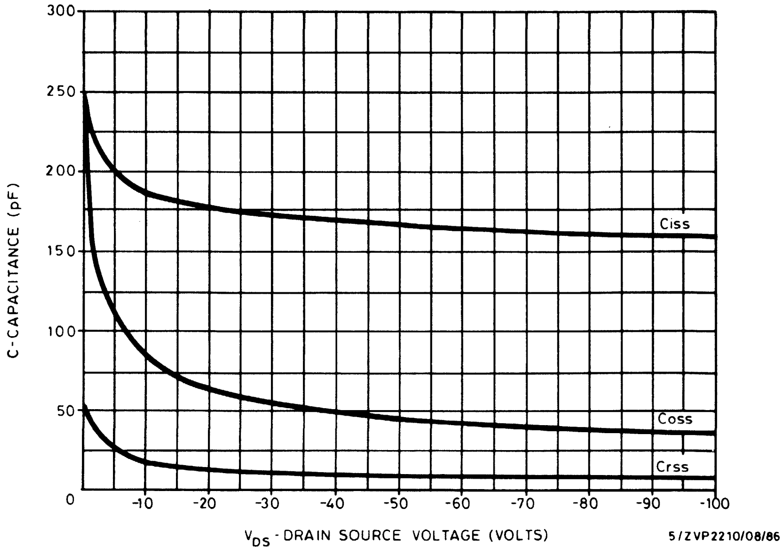


Fig. 5 Typical capacitance v drain-source voltage

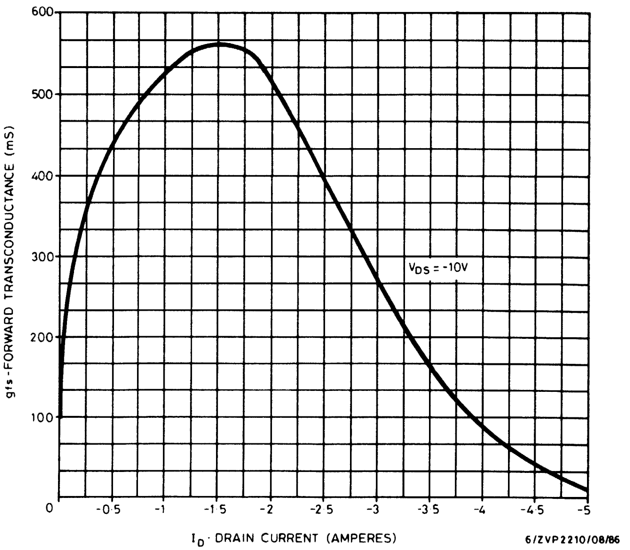


Fig. 6 Typical transconductance v drain current

ZVP2210

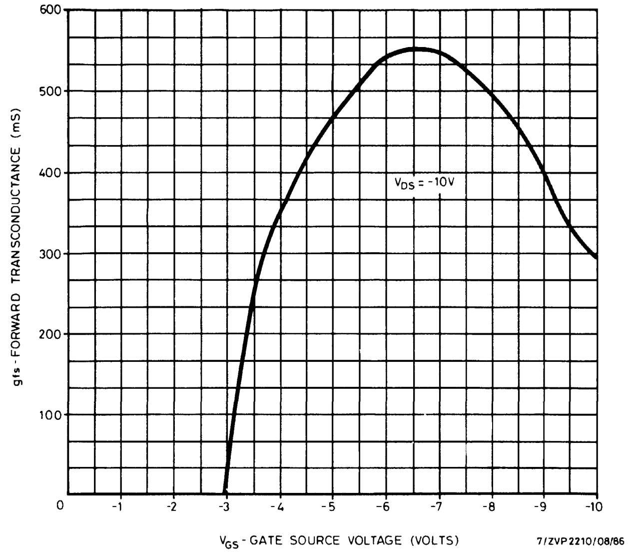


Fig. 7 Typical transconductance v gate-source voltage

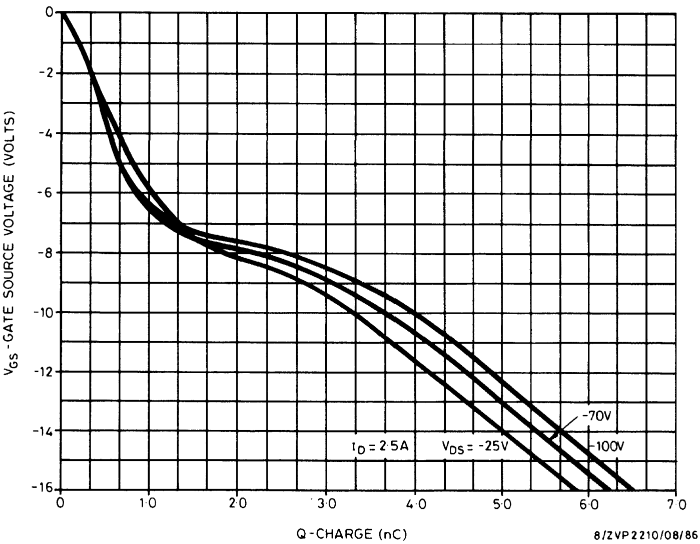


Fig. 8 Typical gate charge v gate-source voltage

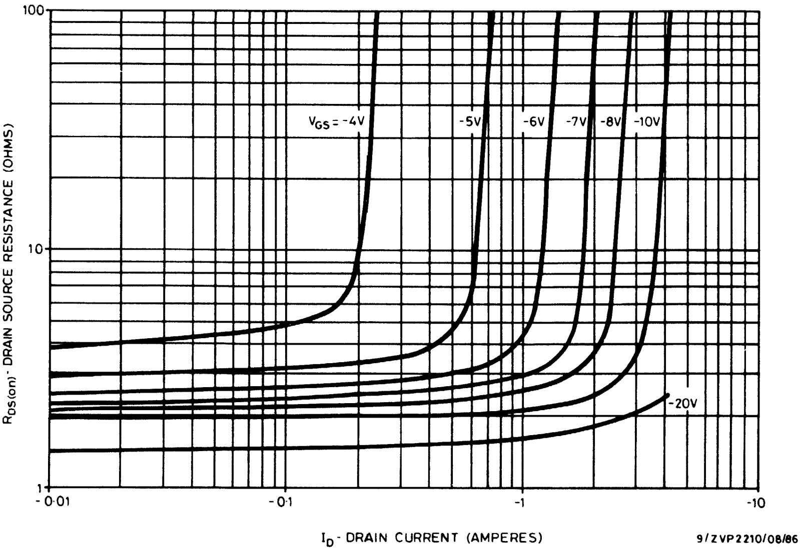


Fig. 9 Typical on-resistance v drain current

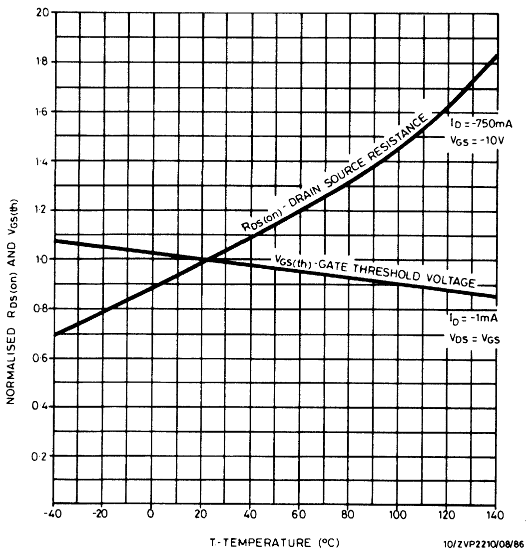


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

ZVP2210

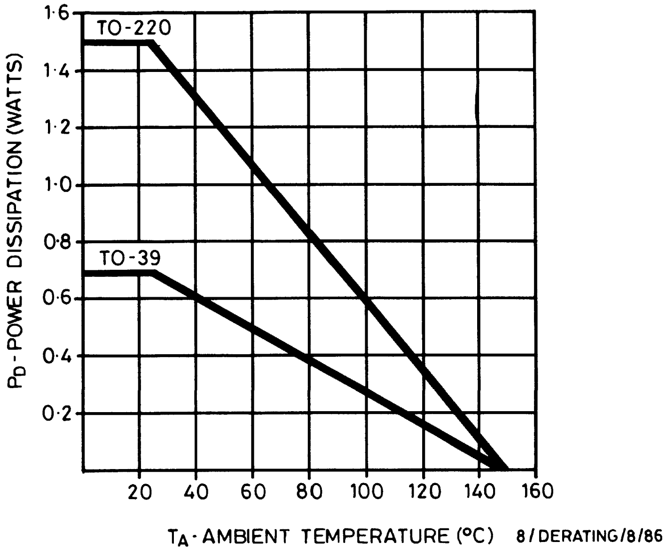


Fig. 11 Power v temperature derating curve (ambient)

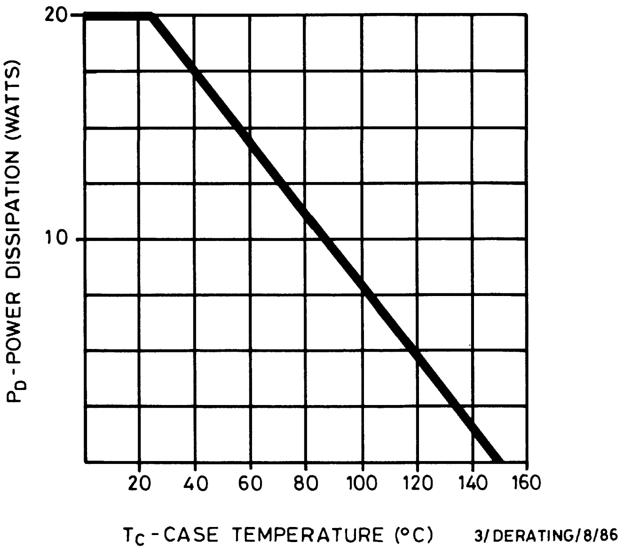


Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

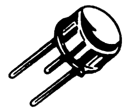
ZVP2220

FEATURES

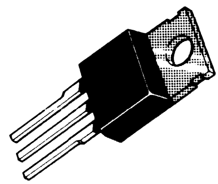
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.



TO-39
SUFFIX B



TO-220
SUFFIX L

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP2220B	−200V	−0.9A	12Ω
ZVP2220L	−200V	−0.9A	12Ω

ZVP2220

ABSOLUTE MAXIMUM RATINGS

	Parameters	TO-39	T0-220	Units
V_{DS}	Drain-source voltage	−200	−200	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.15	−0.23	A
I_D	Continuous drain current (@ $T_C = 25°C$)	−0.9	−0.9	A
I_{DM}	Pulse drain current	−4	−4	A
V_{GS}	Gate-source voltage	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.7	1.5	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	20	20	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150		°C

ELECTRICAL CHARACTERISTICS (at $T = 25°C$ unless otherwise stated)

	Parameter	Min.	Typ.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−200	–	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	–	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate-body leakage	–	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	–	−10	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	–	−200	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	−1	–	–	A	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	–	12	Ω	$I_D = -500mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	–	350	–	mS	$V_{DS} = -25V$, $I_D = -500mA$
C_{iss}	Input capacitance (2)	–	–	240	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–		60	pF	
C_{rss}	Reverse transfer capacitance (2)	–	–	20	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	–	10	ns	$V_{DD} \approx -25V$, $I_D = -500mA$
t_r	Rise time (2) (3)	–	–	20	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	–	25	ns	
t_f	Fall time (2) (3)	–	–	20	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.

(2) Sample test.

(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

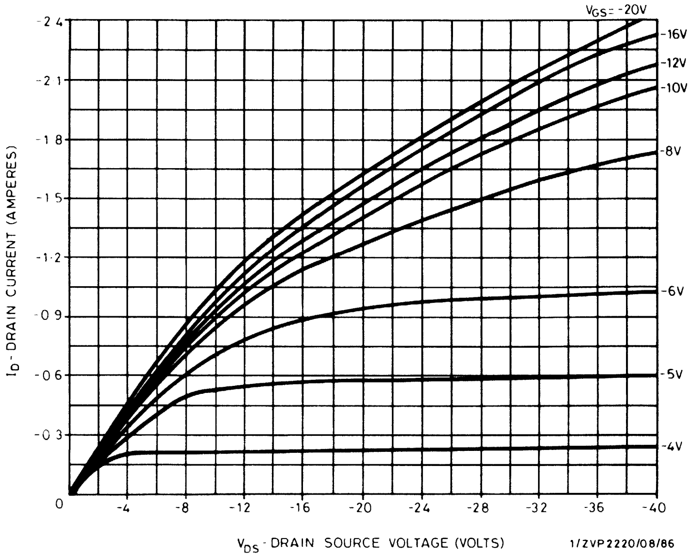


Fig. 1 Typical output characteristics

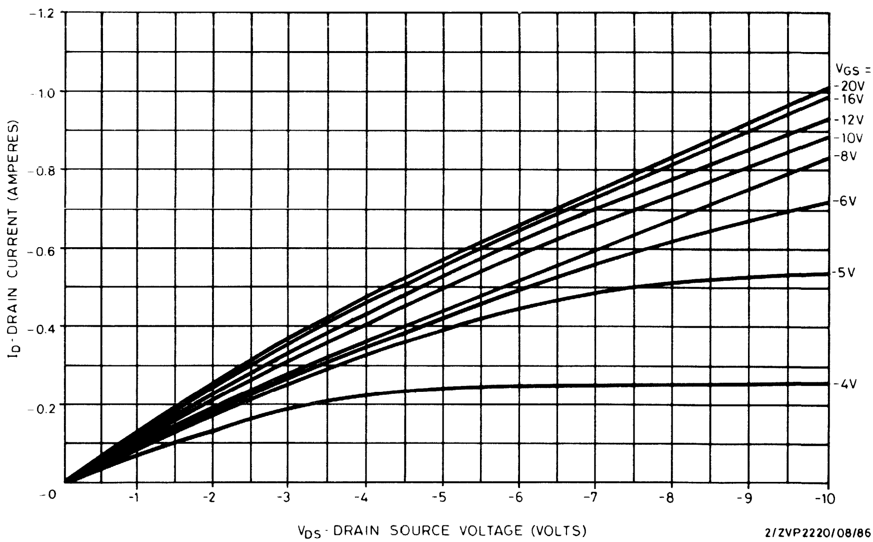


Fig. 2 Typical saturation characteristics

ZVP2220

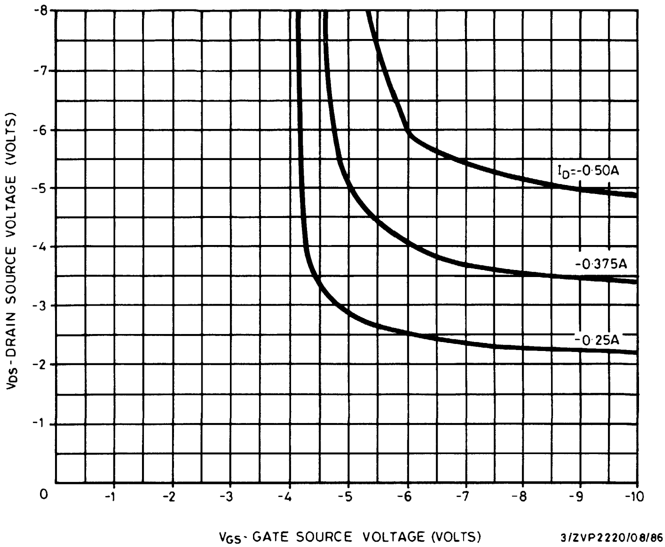


Fig. 3 Typical voltage saturation characteristics

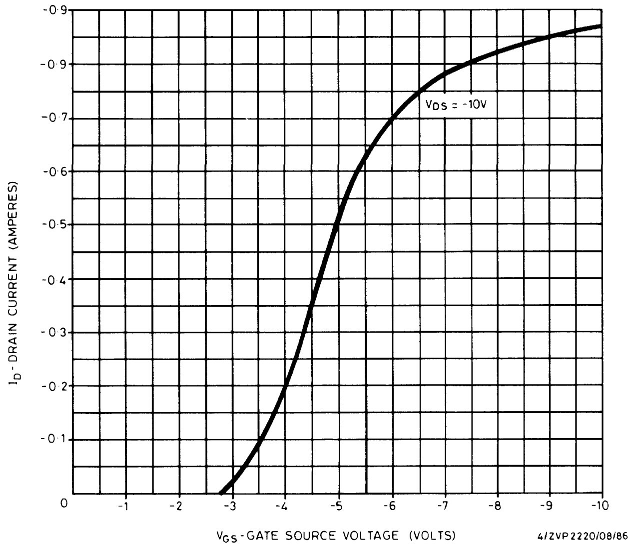


Fig. 4 Typical transfer characteristics

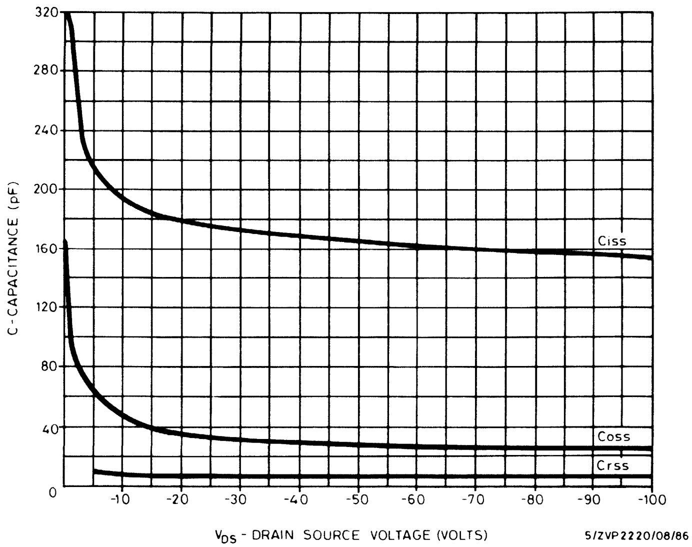


Fig. 5 Typical capacitance v drain-source voltage

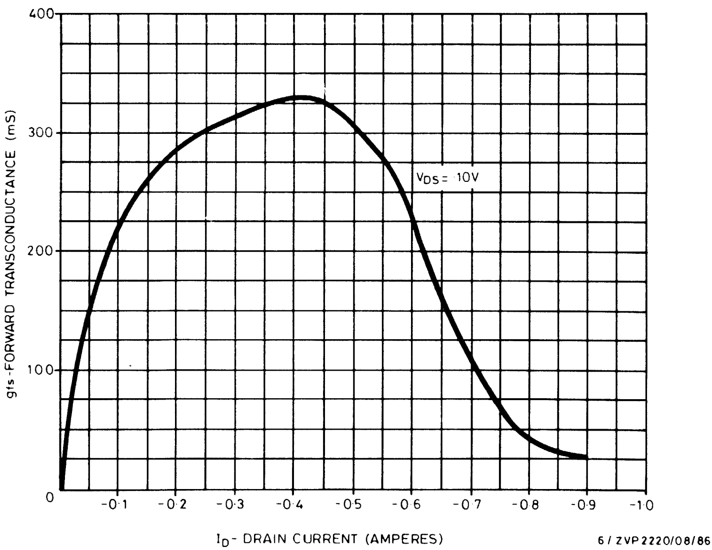


Fig. 6 Typical transconductance v drain current

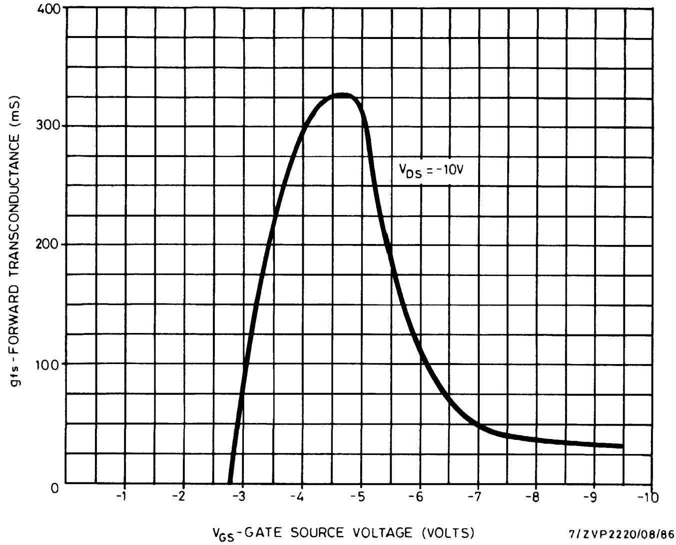


Fig. 7 Typical transconductance v gate-source voltage

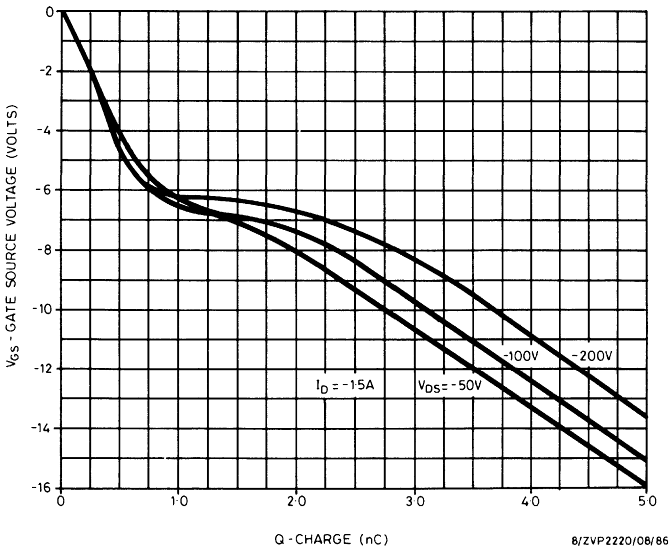


Fig. 8 Typical gate charge v gate-source voltage

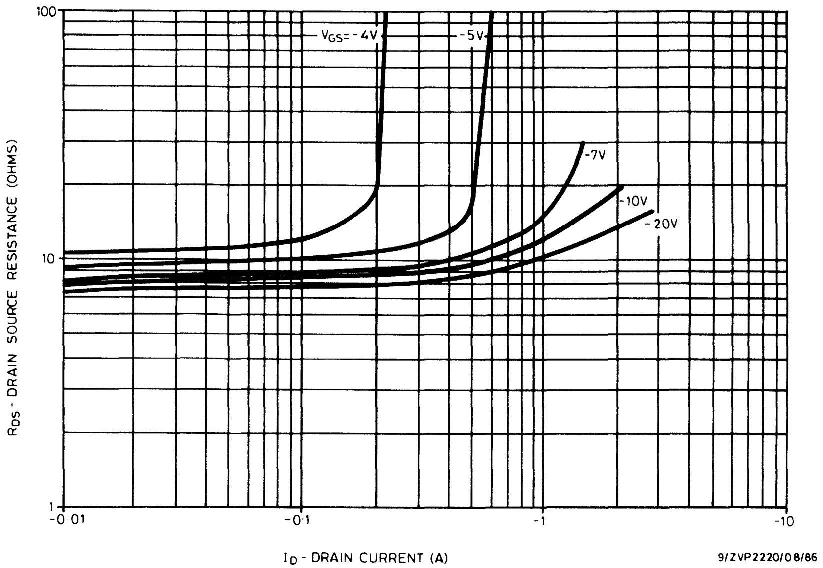


Fig. 9 Typical on-resistance v drain current

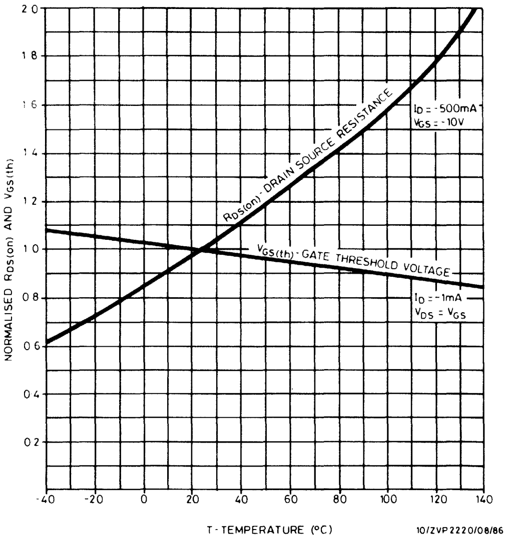


Fig. 10 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

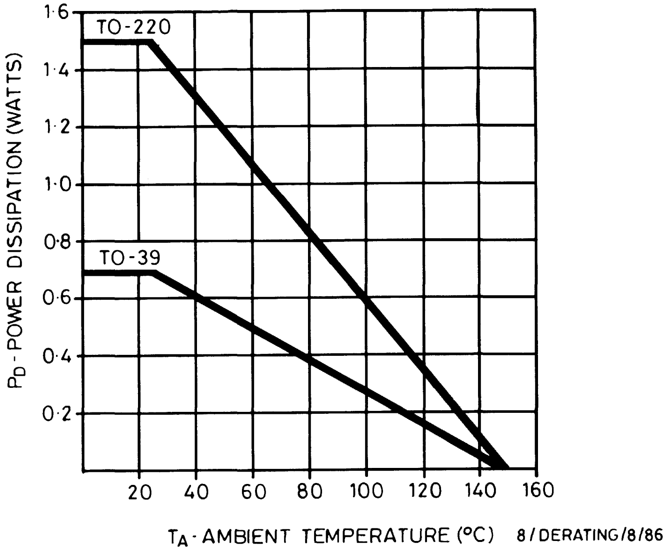


Fig. 11 Power v temperature derating curve (ambient)

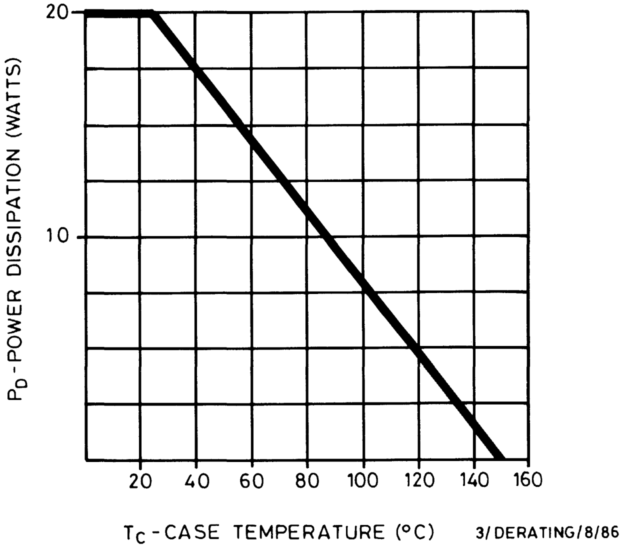
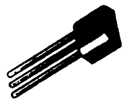


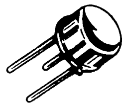
Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

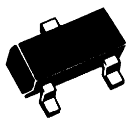
ZVP3306



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



SOT-23
SUFFIX F

FEATURES

- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP3306A	−60V	−0.16A	14Ω
ZVP3306B	−60V	−0.4A	14Ω
ZVP3306F	−60V	−0.09A	14Ω

ZVP3306

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	SOT-23	Units
V_{DS}	Drain-source voltage	−60	−60	−60	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.16	−0.16	−0.09	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.4	–	A
I_{DM}	Pulse drain current	−1.6	−1.6	−1.6	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.625	0.25	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at $T = 25°C$ unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−60	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−0.5	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ ($T = 125°C$) (2)
$I_{D(on)}$	On-state drain current (1)	−400	–	mA	$V_{DS} = -18V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	14	Ω	$I_D = -200mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	60	–	mS	$V_{DS} = -18V$, $I_D = -200mA$
C_{iss}	Input capacitance (2)	–	50	pF	$V_{DS} = -18V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	25	pF	
C_{rss}	Reverse transfer capacitance (2)	–	8	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx -18V$, $I_D = -200mA$
t_r	Rise time (2) (3)	–	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	ns	
t_f	Fall time (2) (3)	–	8	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and <5ns rise time on a pulse generator.

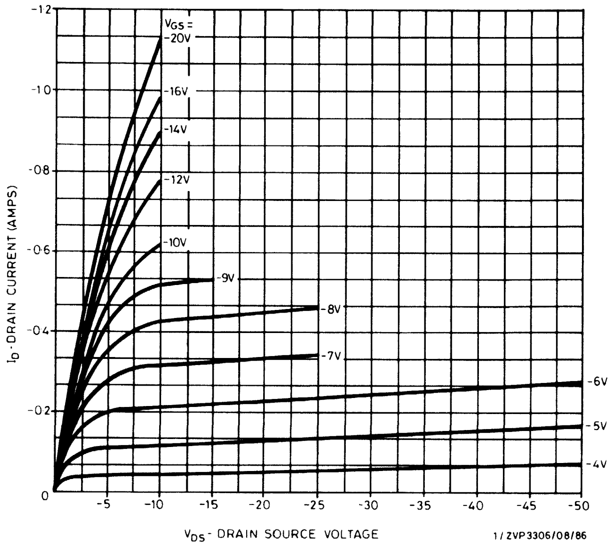


Fig. 1 Typical output characteristics

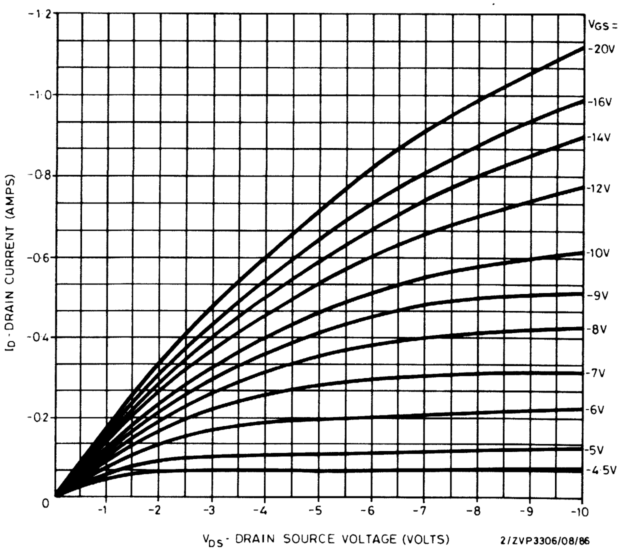


Fig. 2 Typical saturation characteristics

ZVP3306

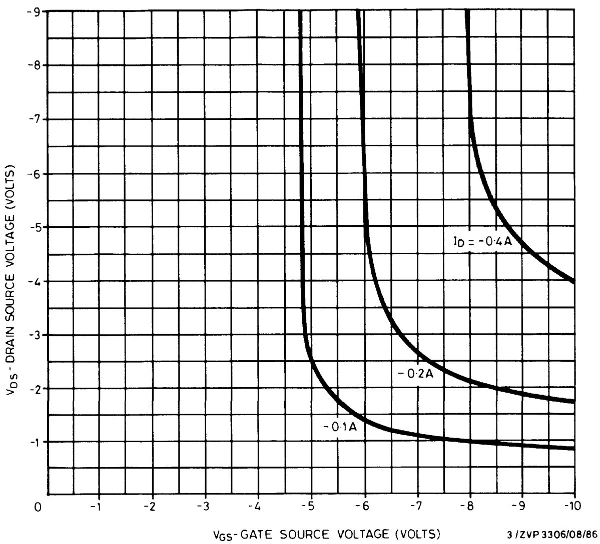


Fig. 3 Typical voltage saturation characteristics

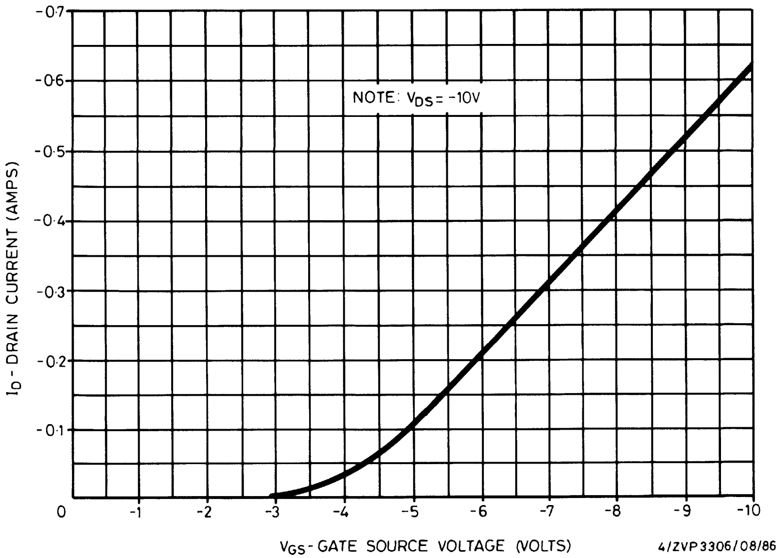


Fig. 4 Typical transfer characteristics

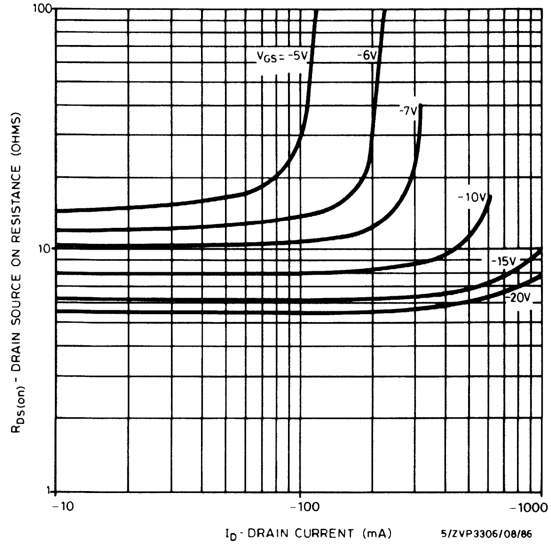


Fig. 5 Typical on-resistance v drain current

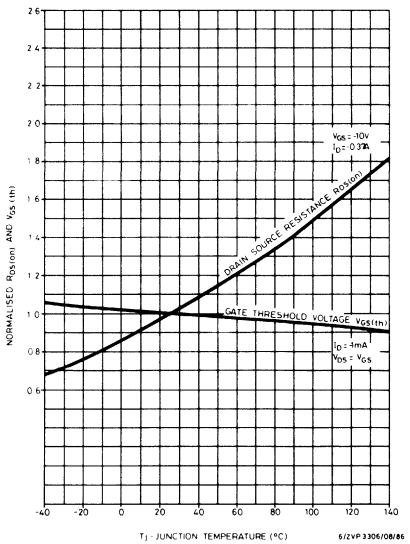


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

ZVP3306

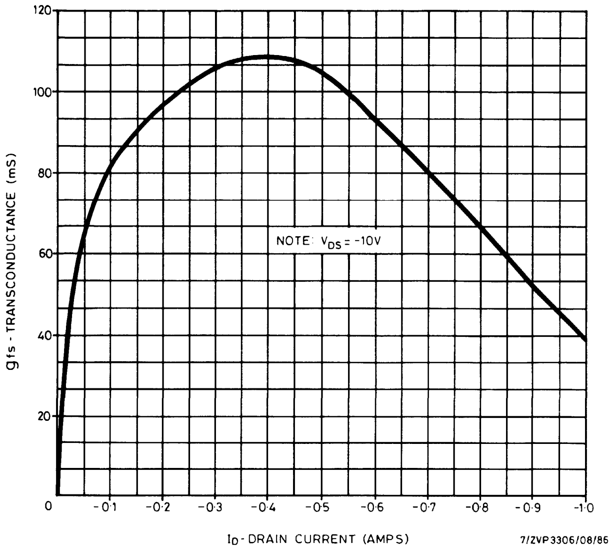


Fig. 7 Typical transconductance v drain current

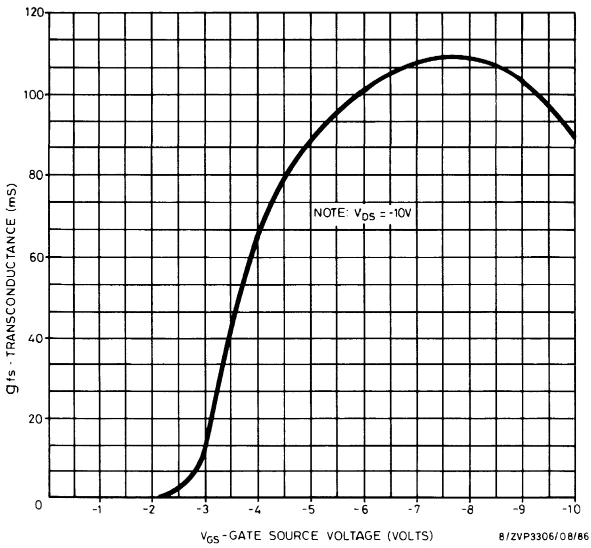


Fig. 8 Typical transconductance v gate-source voltage

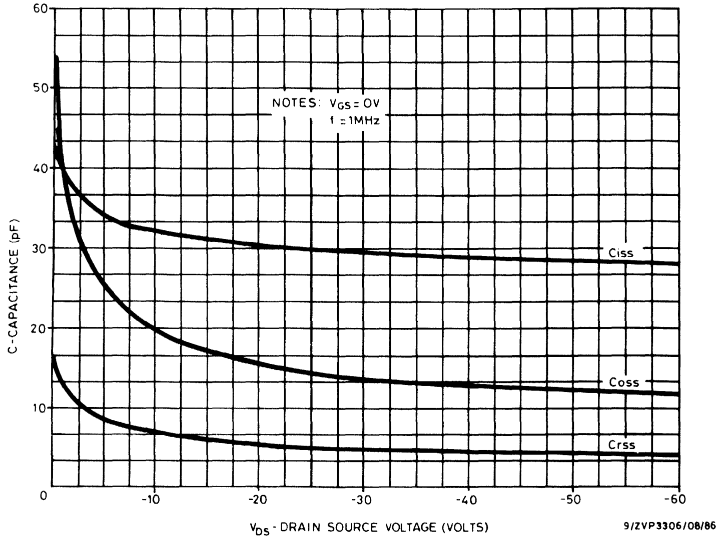


Fig. 9 Typical capacitance v drain-source voltage

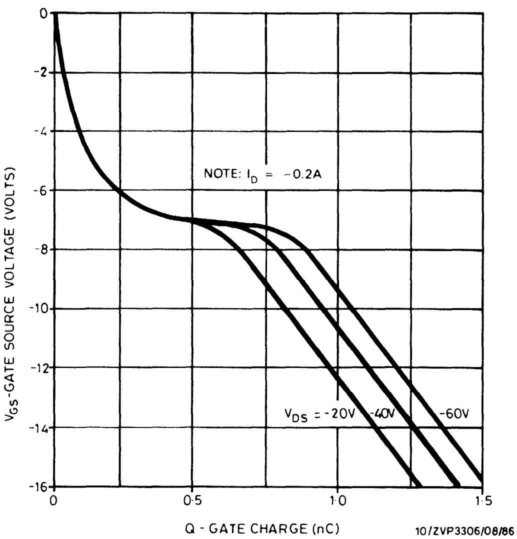


Fig. 10 Typical gate charge v gate-source voltage

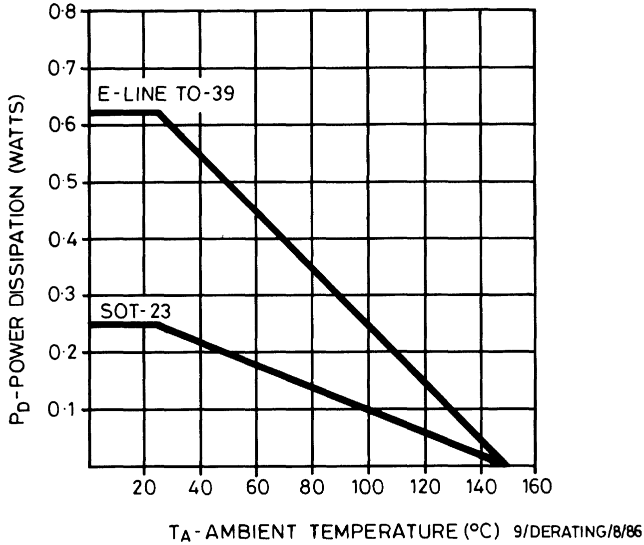


Fig. 11 Power v temperature derating curve (ambient)

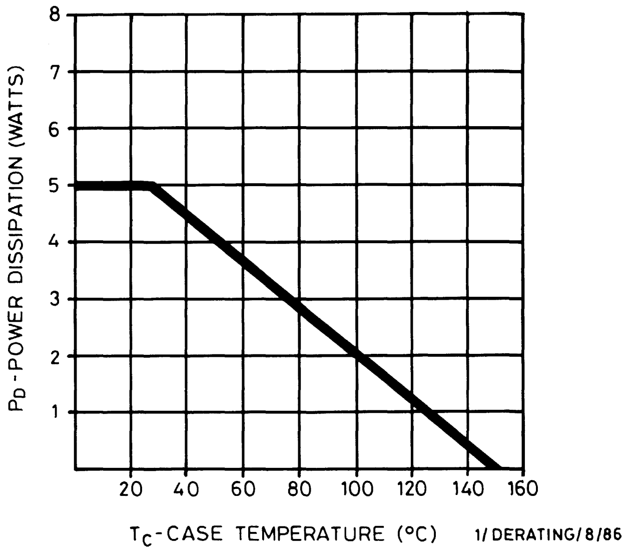


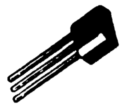
Fig. 12 Power v temperature derating curve (case)

P-channel enhancement mode vertical DMOS FET

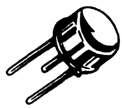
ZVP3310

FEATURES

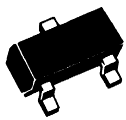
- Compact geometry
- Fast switching speeds
- No secondary breakdown
- Excellent temperature stability
- High input impedance
- Low current drive
- Ease of paralleling



E-LINE (TO-92)
SUFFIX A



TO-39
SUFFIX B



SOT-23
SUFFIX F

DESCRIPTION

A compact interdigitated geometry forms the basis of this Ferranti MOSFET. Optimised for low on-resistance, low capacitance and fast switching this device is manufactured using the latest computer controlled processing techniques in order to achieve greater stability, reliability and ruggedness.

PRODUCT SUMMARY

Part No.	BV_{DSS}	I_D	$R_{DS(on)}$
ZVP3310A	−100V	−0.14A	20Ω
ZVP3310B	−100V	−0.3A	20Ω
ZVP3310F	−100V	−0.075A	20Ω

ZVP3310

ABSOLUTE MAXIMUM RATINGS

	Parameters	E-line	TO-39	SOT-23	Units
V_{DS}	Drain-source voltage	−100	−100	−100	V
I_D	Continuous drain current (@ $T_A = 25°C$)	−0.14	−0.14	−0.075	A
I_D	Continuous drain current (@ $T_C = 25°C$)	–	−0.3	–	A
I_{DM}	Pulse drain current	−1.2	−1.2	−1.2	A
V_{GS}	Gate-source voltage	±20	±20	±20	V
P_D	Max. power dissipation (@ $T_A = 25°C$)	0.625	0.625	0.25	W
P_D	Max. power dissipation (@ $T_C = 25°C$)	–	5	–	W
T_j, T_{stg}	Operating/storage temperature range	−55 to +150			°C

ELECTRICAL CHARACTERISTICS (at T = 25°C unless otherwise stated)

	Parameter	Min.	Max.	Unit	Conditions
BV_{DSS}	Drain-source breakdown voltage	−100	–	V	$I_D = -1mA$, $V_{GS} = 0V$
$V_{GS(th)}$	Gate-source threshold voltage	−1.5	−3.5	V	$I_D = -1mA$, $V_{DS} = V_{GS}$
I_{GSS}	Gate body leakage	–	20	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	–	−1	μA	V_{DS} = Max. rating, $V_{GS} = 0V$
		–	−50	μA	$V_{DS} = 0.8 \times$ Max. rating $V_{GS} = 0V$ (T = 125°C) (2)
$I_{D(on)}$	On-state drain current (1)	−300	–	mA	$V_{DS} = -25V$, $V_{GS} = -10V$
$R_{DS(on)}$	Static drain-source on-state resistance (1)	–	20	Ω	$I_D = -150mA$, $V_{GS} = -10V$
g_{fs}	Forward transconductance (1) (2)	50	–	mS	$V_{DS} = -25V$, $I_D = -150mA$
C_{iss}	Input capacitance (2)	–	50	pF	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz
C_{oss}	Common source output capacitance (2)	–	15	pF	
C_{rss}	Reverse transfer capacitance (2)	–	5	pF	
$t_{d(on)}$	Turn-on delay time (2) (3)	–	8	ns	$V_{DD} \approx -25V$, $I_D = -150mA$
t_r	Rise time (2) (3)	–	8	ns	
$t_{d(off)}$	Turn-off delay time (2) (3)	–	8	ns	
t_f	Fall time (2) (3)	–	8	ns	

(1) Measured under pulsed conditions. Width = 300μs. Duty cycle ≤ 2%.
(2) Sample test.
(3) Switching times measured with 50Ω source impedance and < 5ns rise time on a pulse generator.

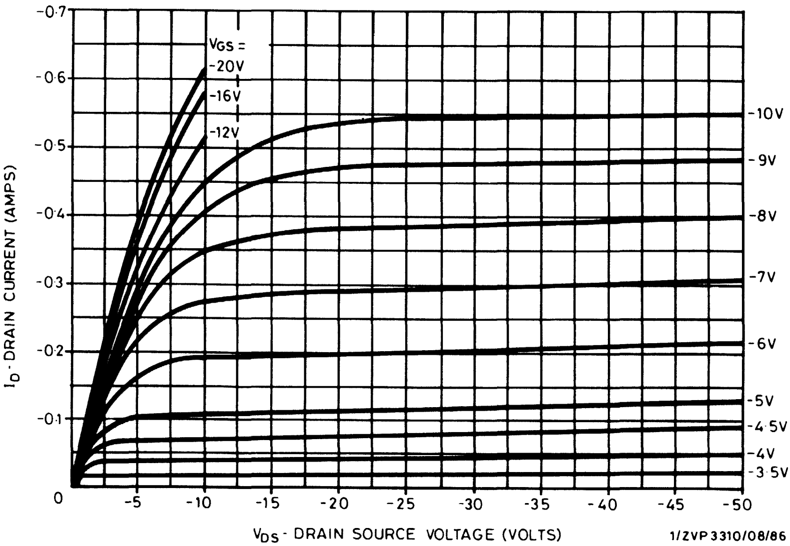


Fig. 1 Typical output characteristics

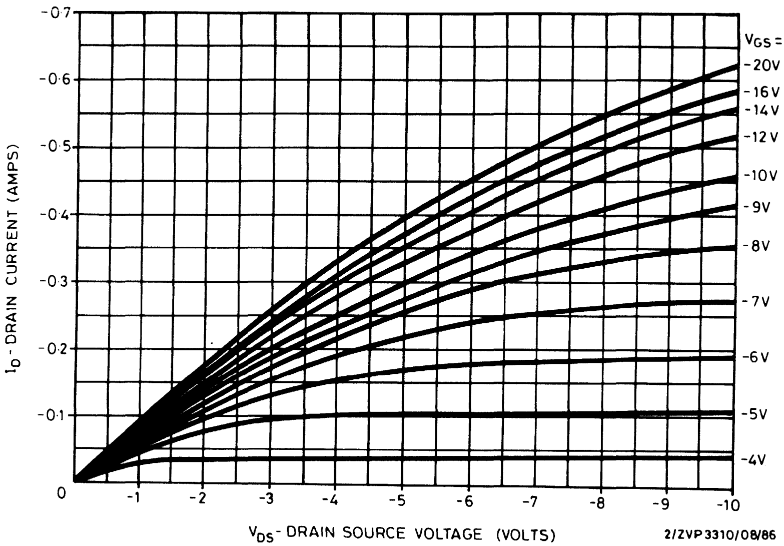


Fig. 2 Typical saturation characteristics

ZVP3310

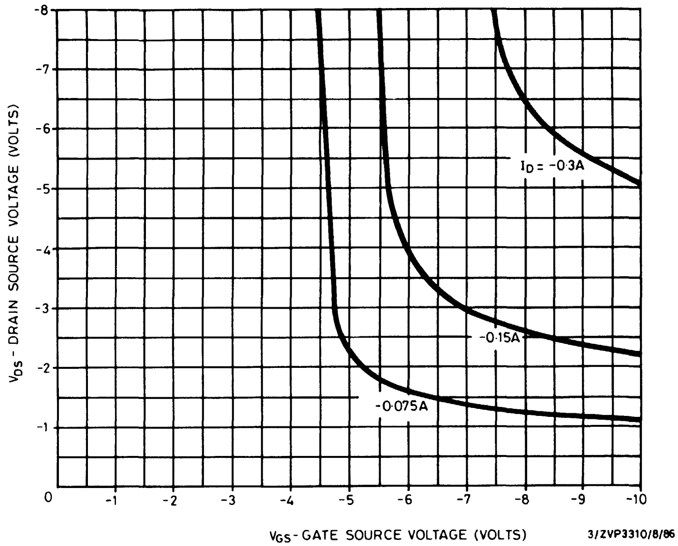


Fig. 3 Typical voltage saturation characteristics

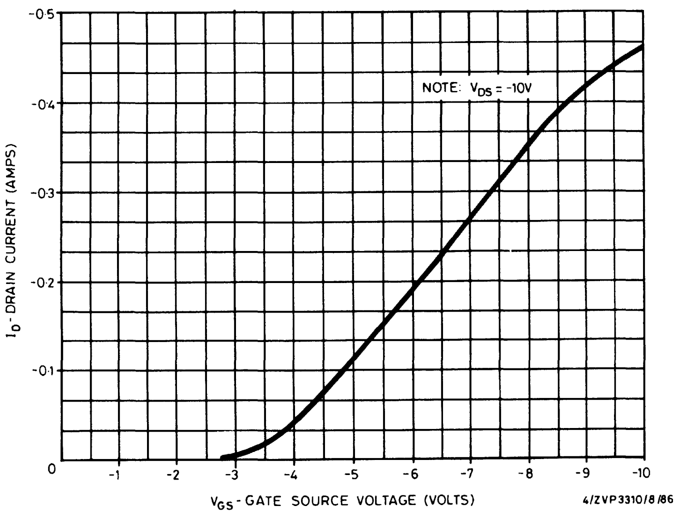


Fig. 4 Typical transfer characteristics

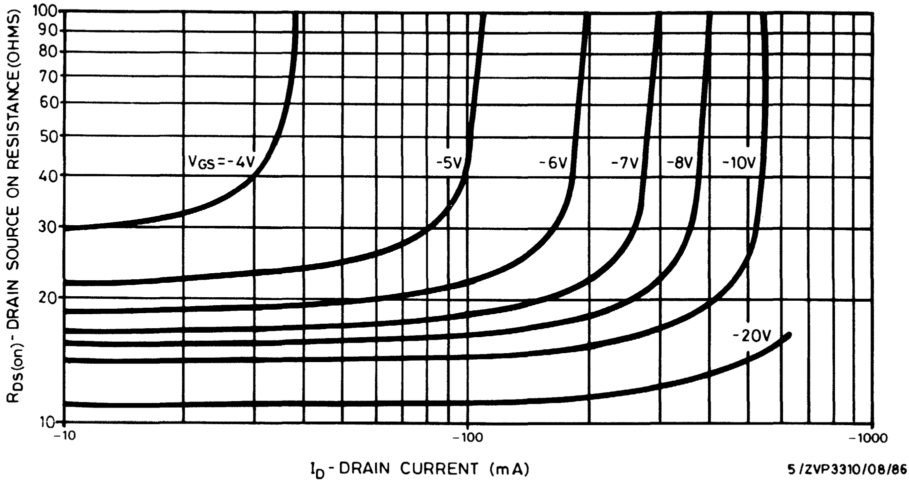


Fig. 5 Typical on-resistance v drain current

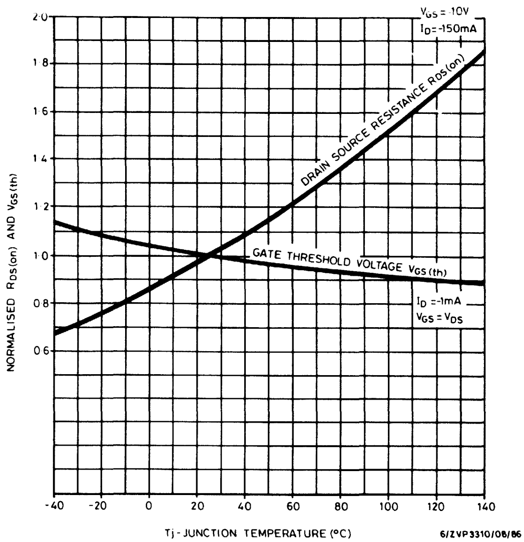


Fig. 6 Normalised $R_{DS(on)}$ and $V_{GS(th)}$ v temperature

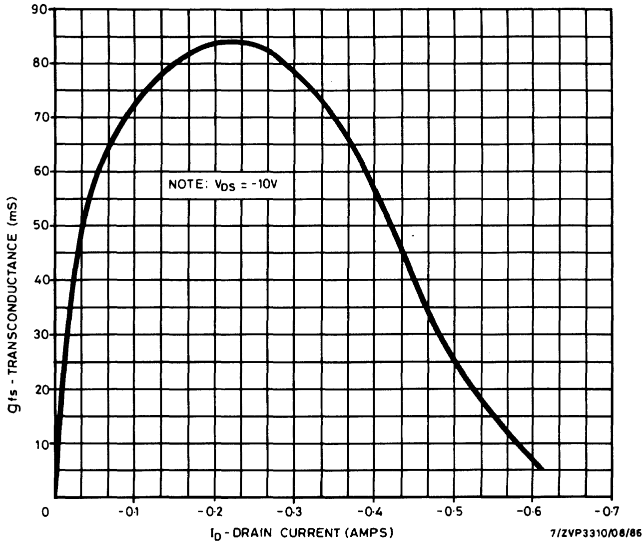


Fig. 7 Typical transconductance v drain current

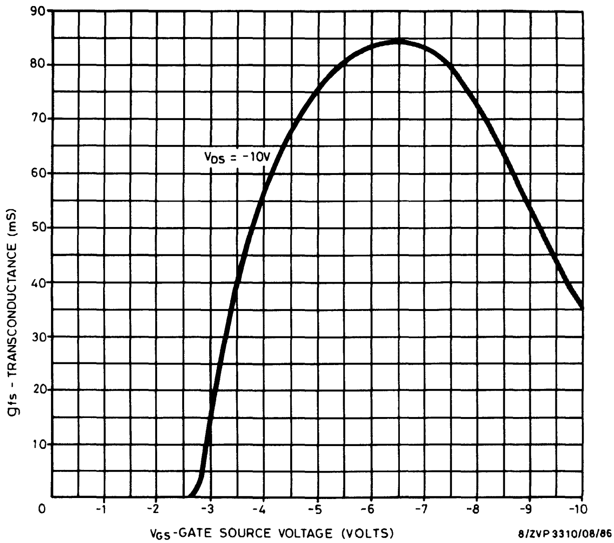


Fig. 8 Typical transconductance v gate-source voltage

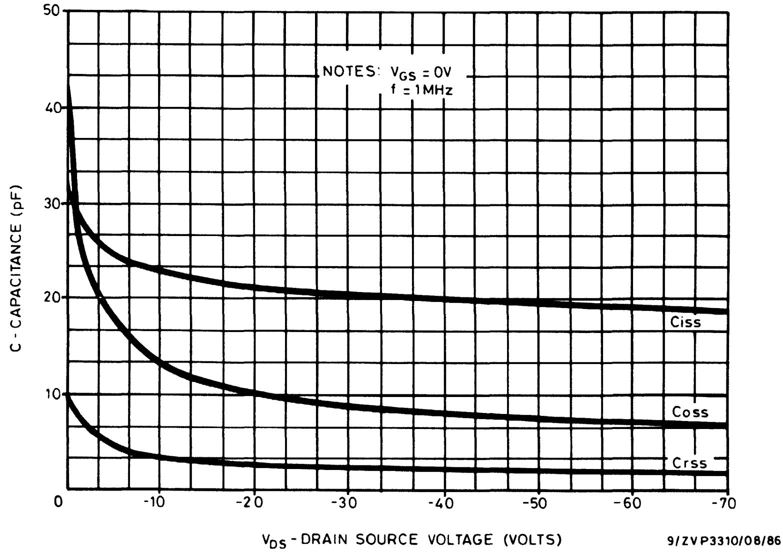


Fig. 9 Typical capacitance v drain-source voltage

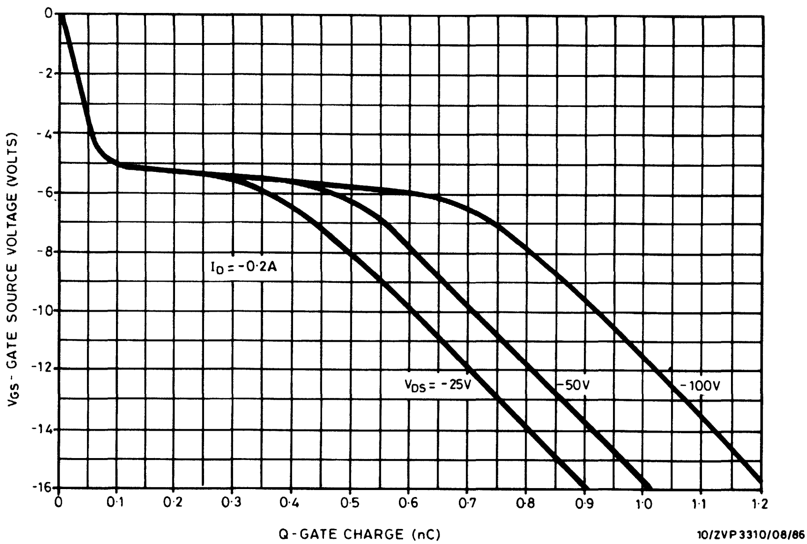


Fig. 10 Typical gate charge v gate-source voltage

ZVP3310

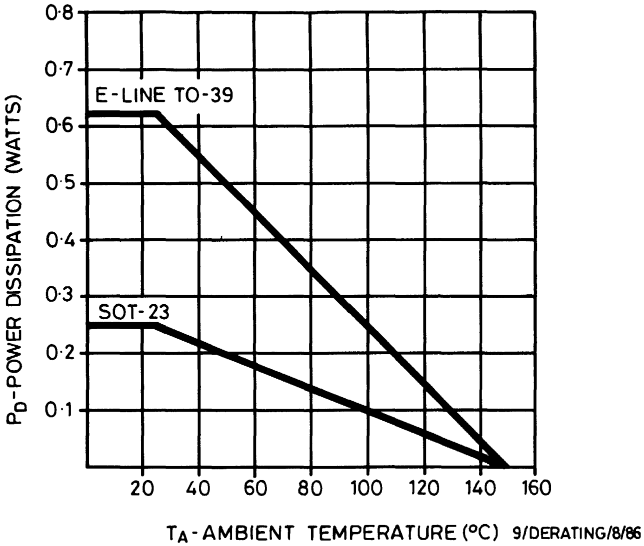


Fig. 11 Power v temperature derating curve (ambient)

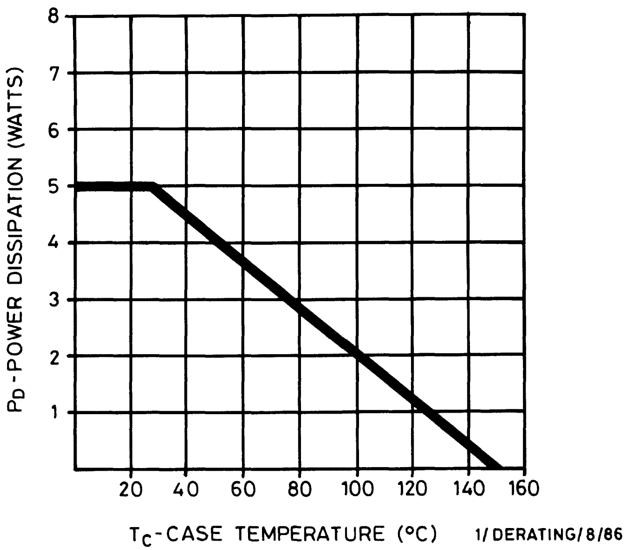
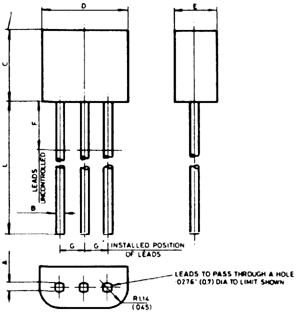


Fig. 12 Power v temperature derating curve (case)

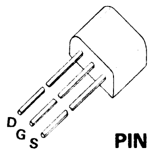
PACKAGE OUTLINE AND PIN OUT

PACKAGE DETAILS

E-Line (TO-92 style)



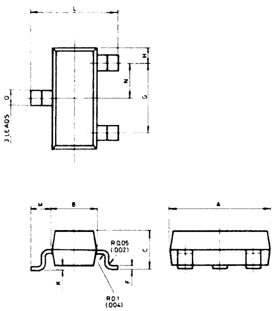
DIMENSION	MILLIMETRES		INCHES	
	MIN	MAX	MIN	MAX
A	0.41	0.495	0.016	0.0195
B	0.41	4.01	0.016	0.0195
C	3.61	4.01	0.142	0.158
D	4.37	4.77	0.172	0.188
E	2.16	2.41	0.085	0.095
F		2.5		0.098
G	1.27 NOM		0.050 NOM	
L	12.06	13.97	0.475	0.550



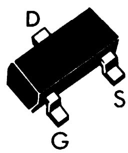
PIN CONFIGURATION

Available on tape on reels. Please enquire for details.

SOT-23



DIMENSION	MILLIMETRES		INCHES	
	MIN	MAX	MIN	MAX
A	2.75	3.04	0.108	0.120
B	1.2	1.4	0.047	0.055
C	0.89	1.12	0.035	0.044
D	0.37	0.43	0.0145	0.017
F	0.085	0.14	0.0034	0.0055
G	1.78	2.04	0.070	0.080
H	0.33	0.51	0.013	0.020
K	0.075	0.125	0.003	0.005
L	2.10	2.5	0.0825	0.0985
M	0.45	0.64	0.018	0.025
N	0.89	1.02	0.035	0.040

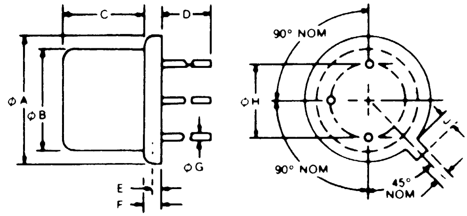


PIN CONFIGURATION

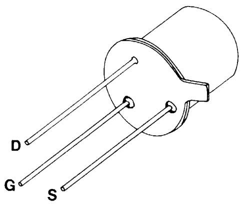
Available in tape on reels. Please enquire for details.

PACKAGE DETAILS

TO-39

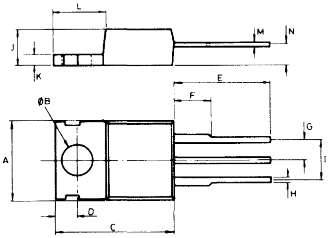


DIMENSION	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
∅A	350	370	8.99	9.40
∅B	306	335	7.77	8.51
C	240	260	6.10	6.60
D	500		12.70	
E	009	023	229	548
F	018	045	458	1.143
∅G	016	021	406	533
∅H	190	210	4.83	5.33
I	028	037	711	939
J	026	040	660	1.016

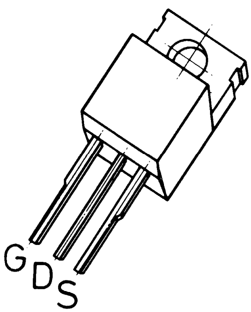


PIN CONFIGURATION

TO-220



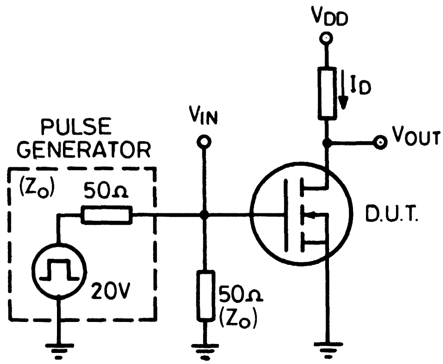
DIMENSION	INCHES		MILLIMETRES	
	MIN	MAX	MIN	MAX
A	0.387	0.403	9.8	10.2
∅B	0.139	0.147	3.53	3.73
C	0.612	0.648	15.56	16.46
D	0.10	0.12	2.55	3.05
E	0.50	0.56	12.71	14.21
F		0.25		6.35
G	0.09	0.11	2.29	2.79
H	0.022	0.032	0.57	0.83
I	0.19	0.21	4.85	5.35
J	0.17	0.19	4.32	4.82
K	0.045	0.055	1.14	1.4
L	0.245	0.265	6.23	6.73
M	0.015	0.025	0.37	0.63
N	0.085	0.105	2.15	2.65



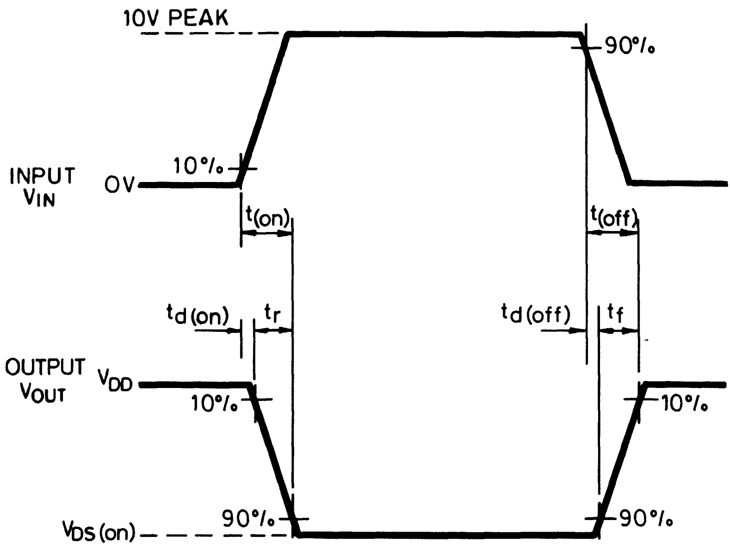
PIN CONFIGURATION

SWITCHING CIRCUITS
AND
WAVEFORMS

N-channel



Circuit for measuring switching speed

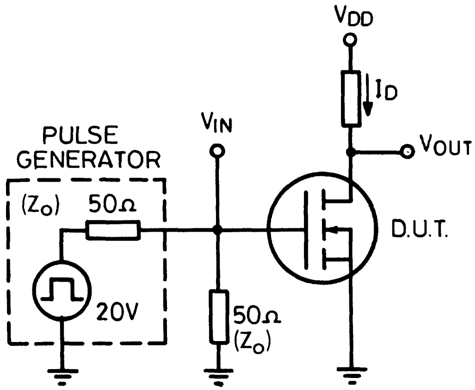


N/MOS/H/B/08/86

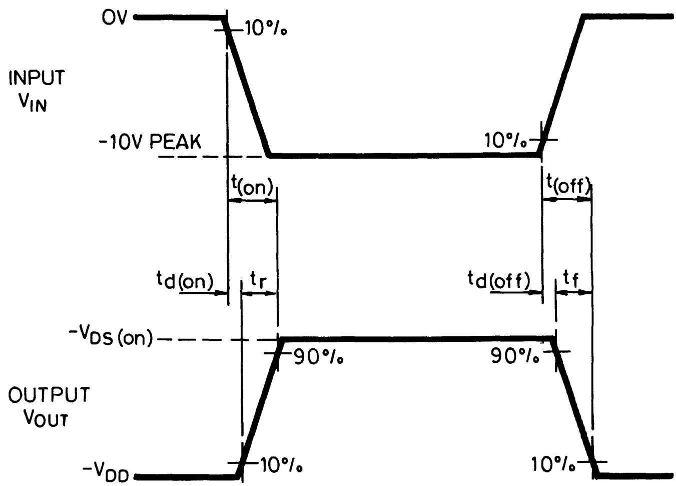
Waveforms

SWITCHING

P-channel



Circuit for measuring switching speed



P/MOS/H/B/08/86

Waveforms

NOTES

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